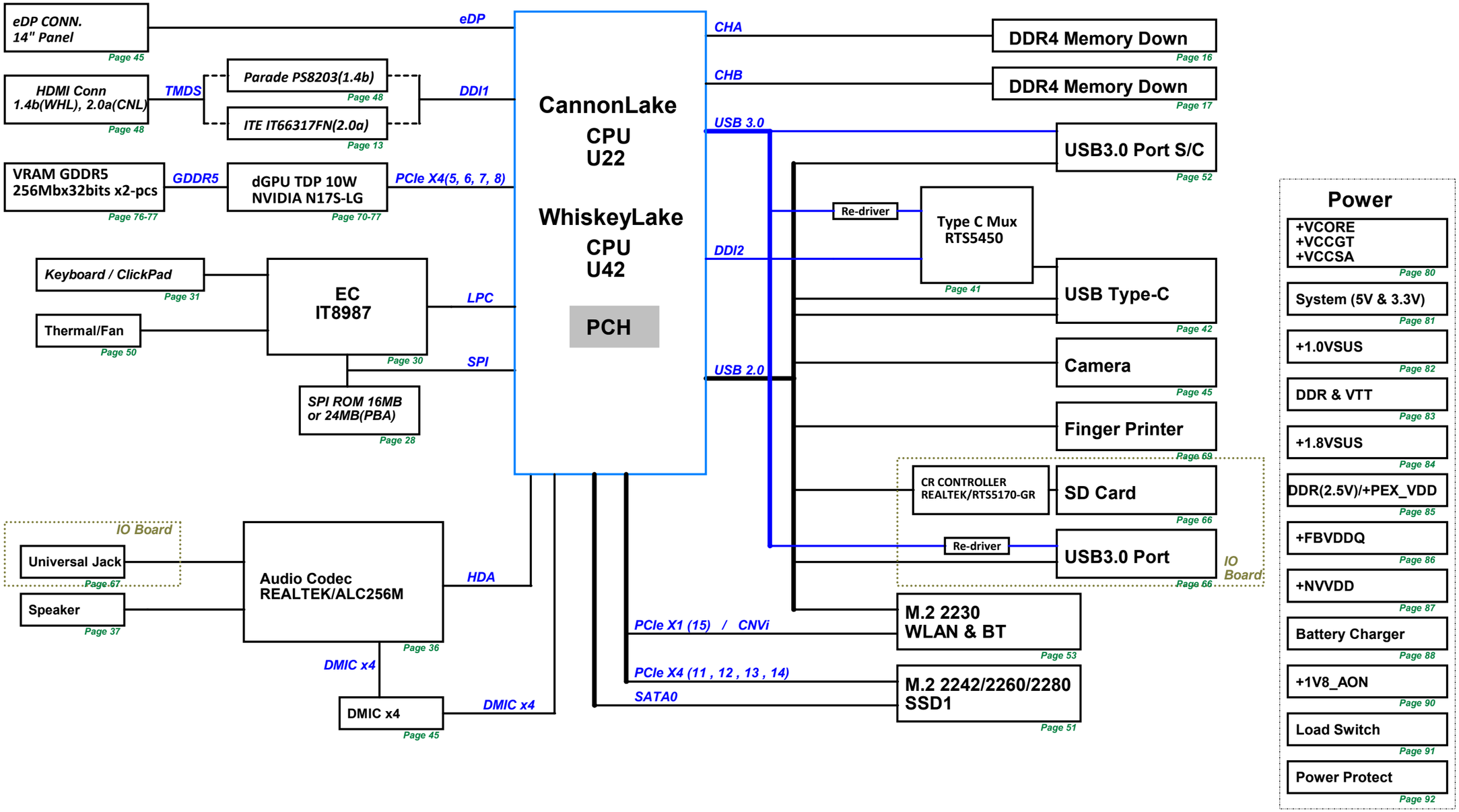
Miller with Intel WHL/CNL

Block Diagram



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Title : Block Diagram

BG1-HW3 RD

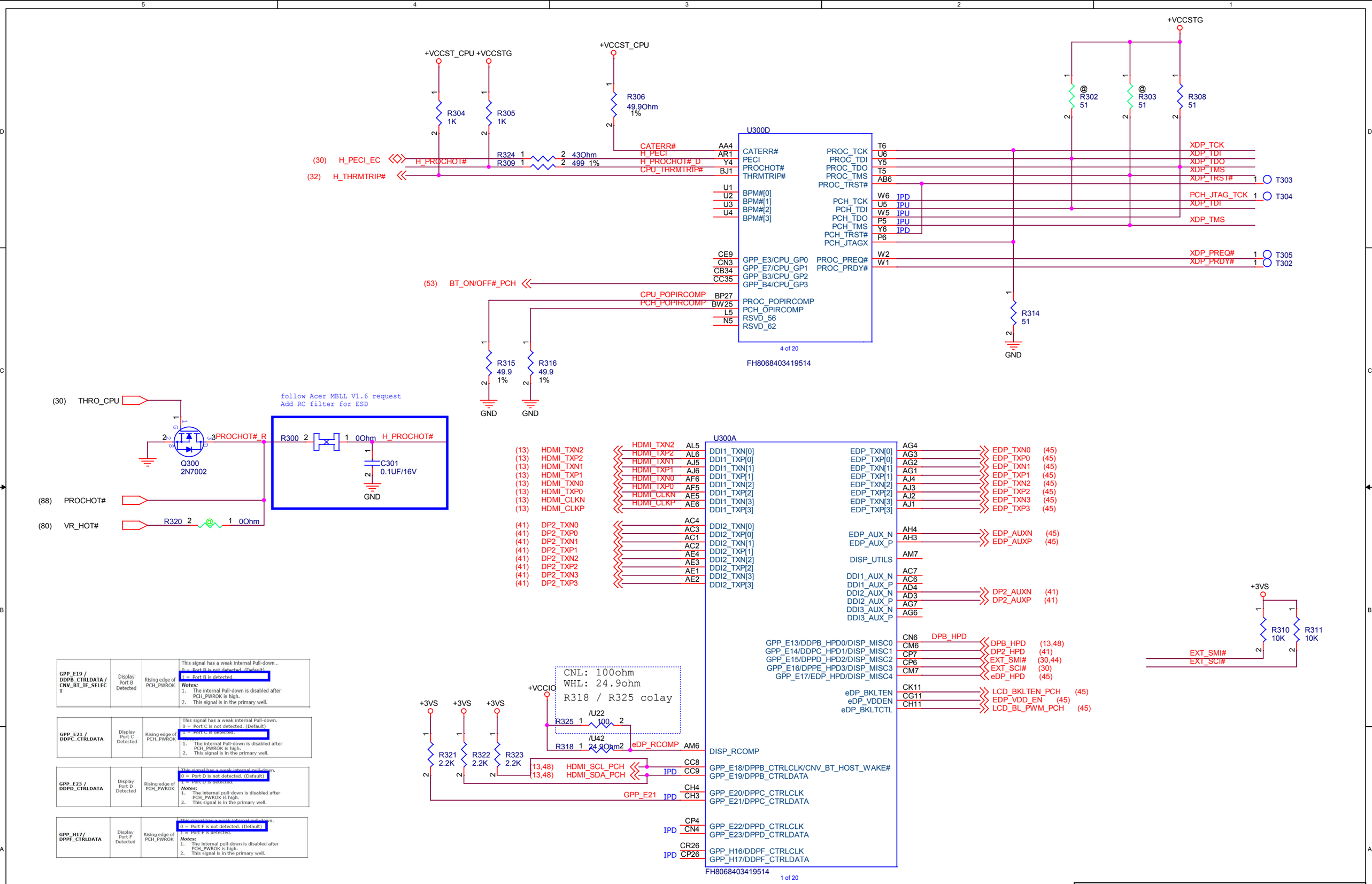
Engineer: Howard Chen

Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 1 of 94

Option

Optional	Remark
@	Ummount
/Debug	Debug only
/EMI	Reserved EMI part
/UMA	Support UMA
/VGA	Support VGA
/U22	Support 2+2 CPU
/U42	Support 4+2 CPU
/TPM	Support TPM function



GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. *Notes:* 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. *Notes:* 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. *Notes:* 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17/ DDPF_CTRLDATA	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. *Notes:* 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

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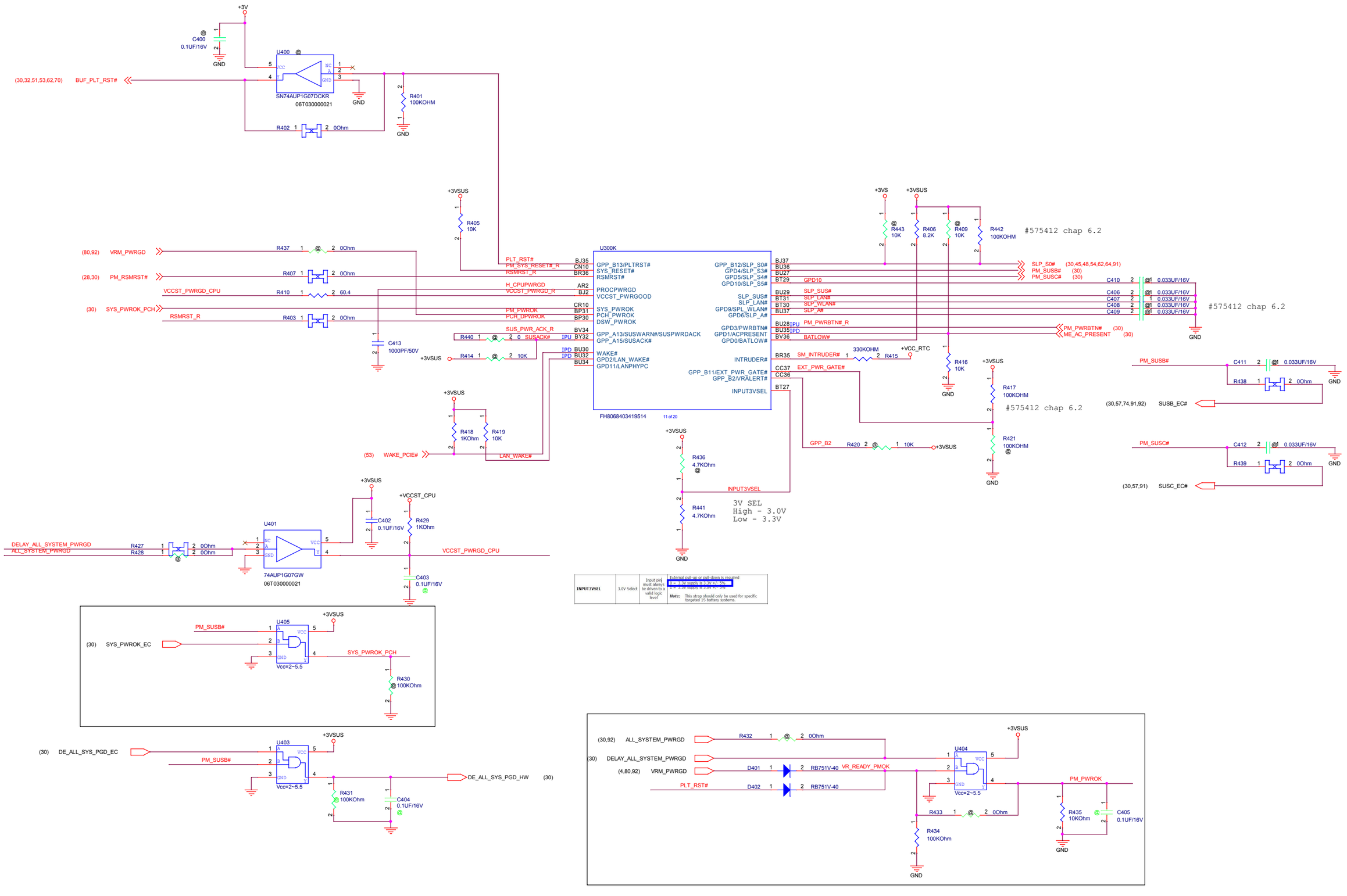
Title: MISC,JTAG,DDI,EDP

Engineer: Howard_Chen

Size	Project Name	Rev
A3	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 3 of 94



INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 1 = 3.3V supply is 3.0V +/- 5% 1 = 3.3V supply is 3.0V +/- 3% **Note:** This strap should only be used for specific targeted 1S battery systems.

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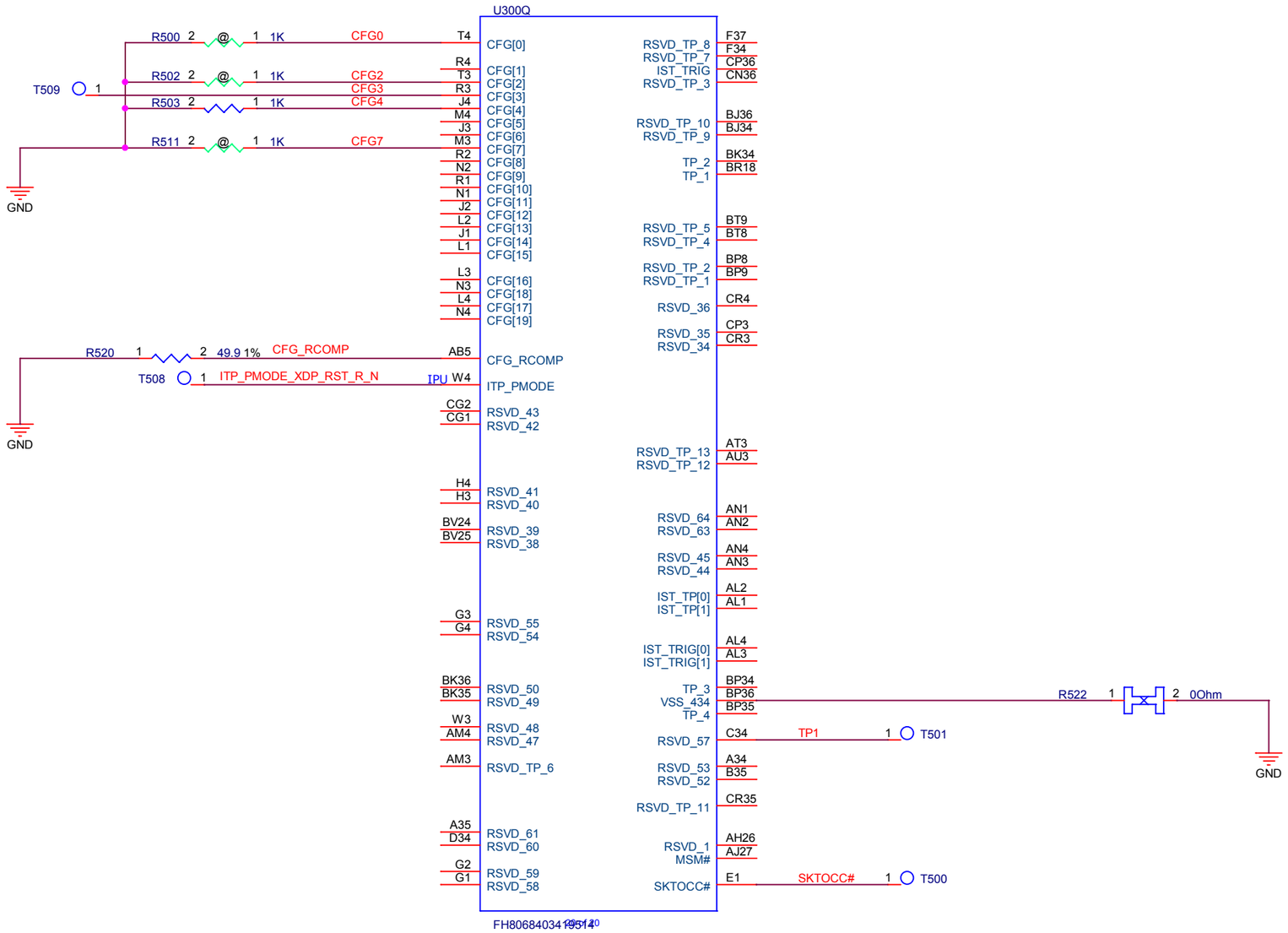
Title : CPU_SYS_POWER_MANAGER
Engineer: Howard_Chen
Size A2
Project Name MILLER
Rev 1.4
Date: Monday, June 11, 2018
Sheet 4 of 94

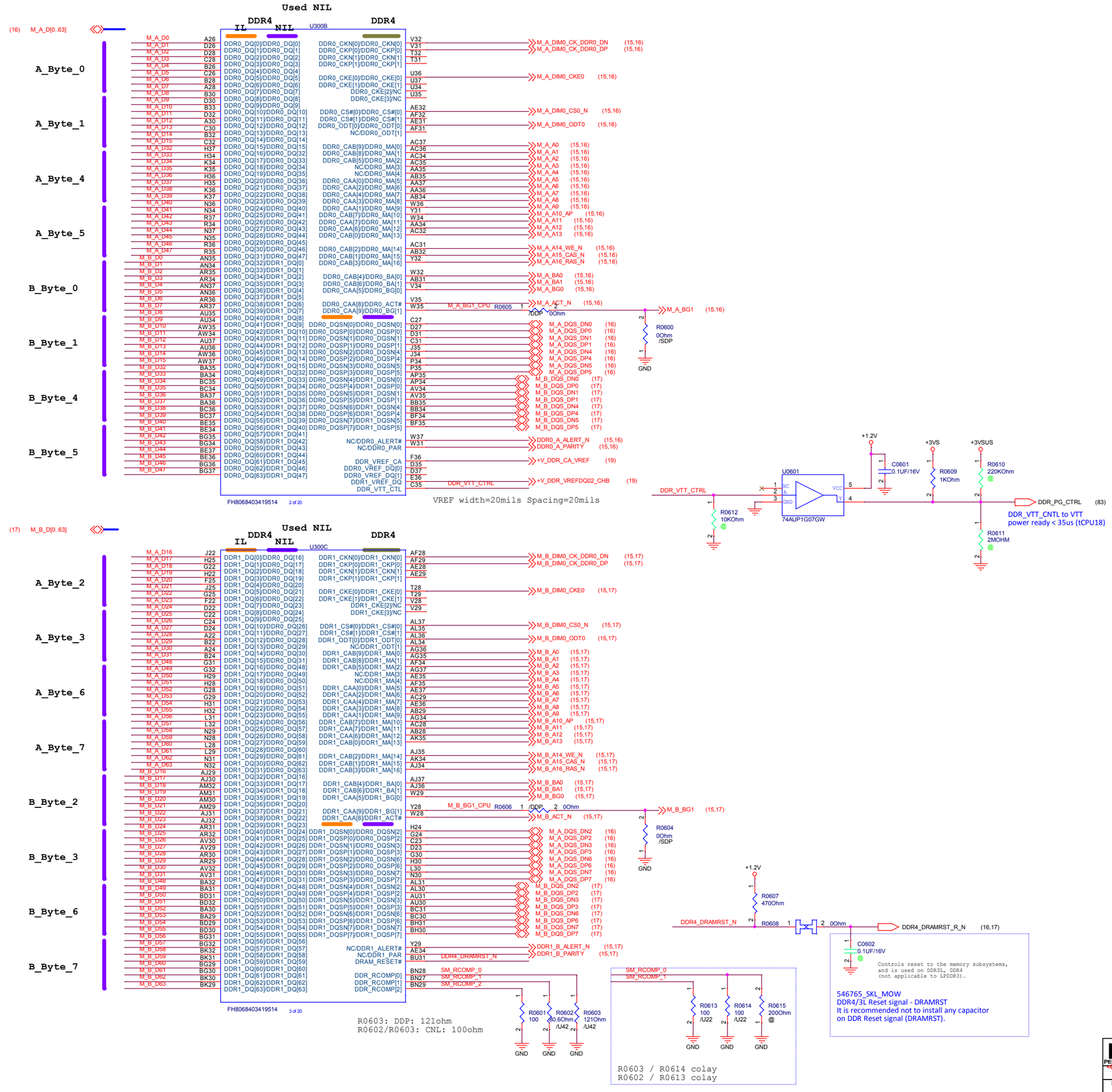
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[3:1]**: Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[19:5]:** Reserved configuration lanes.	I	GTL	SE	All Processor Lines.



PEGATRON Title: CPU_RESERVED
PEGATRON PROPRIETARY AND CONFIDENTIAL
<OrgName>
Engineer: Howard_Chen

Size	Project Name	Rev
A3	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 5 of 94



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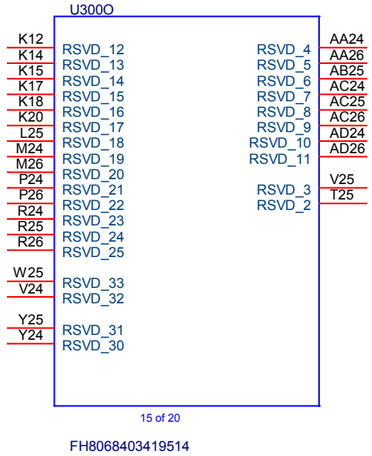
Original

Title : CPU_DDR4

Engineer: Howard_Chen

Size	Project Name	Rev
A2	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 6 of 34



FH8068403419514

PEGATRON

Title : CPU_RSVD

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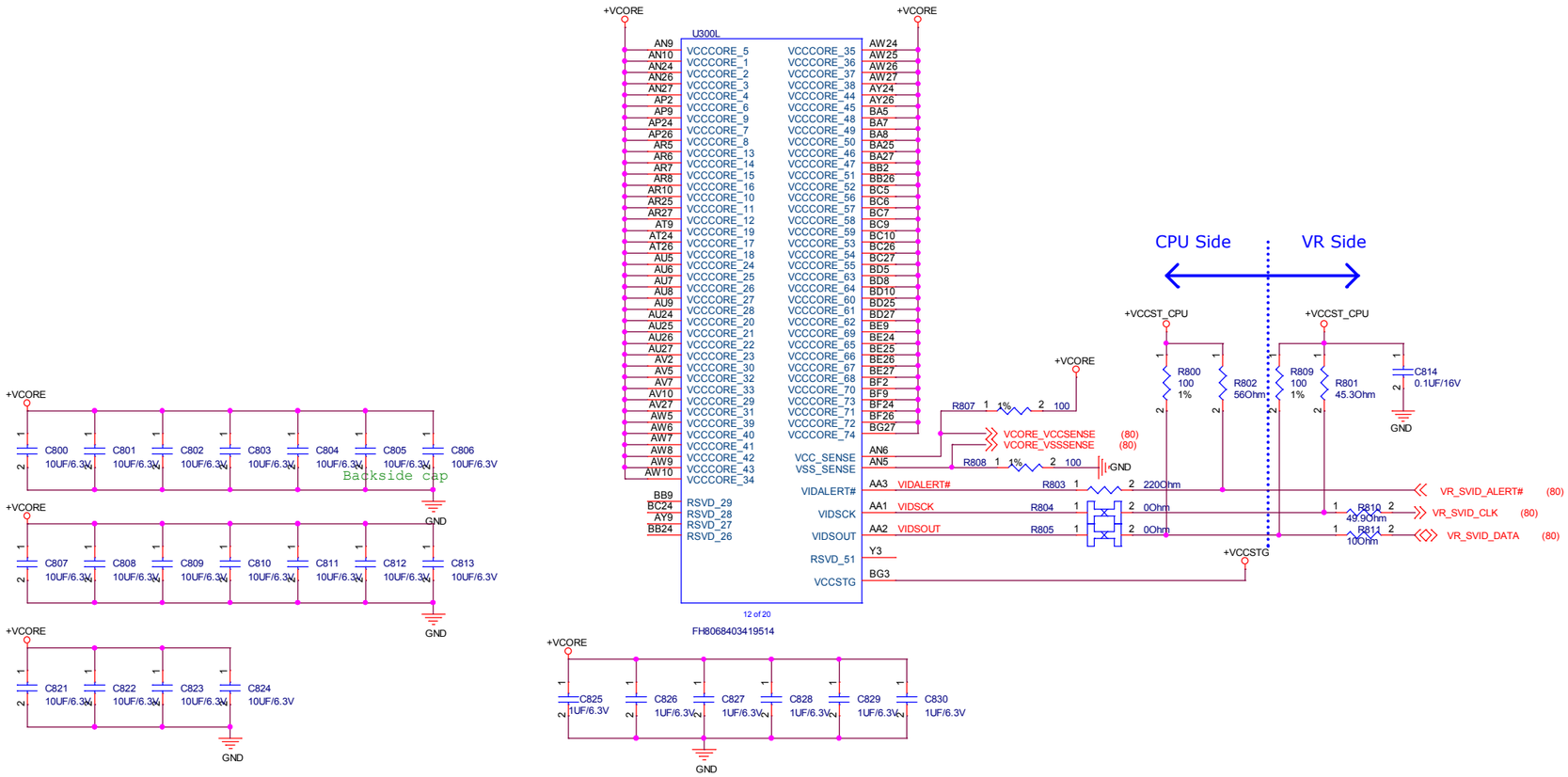
<OrgName>

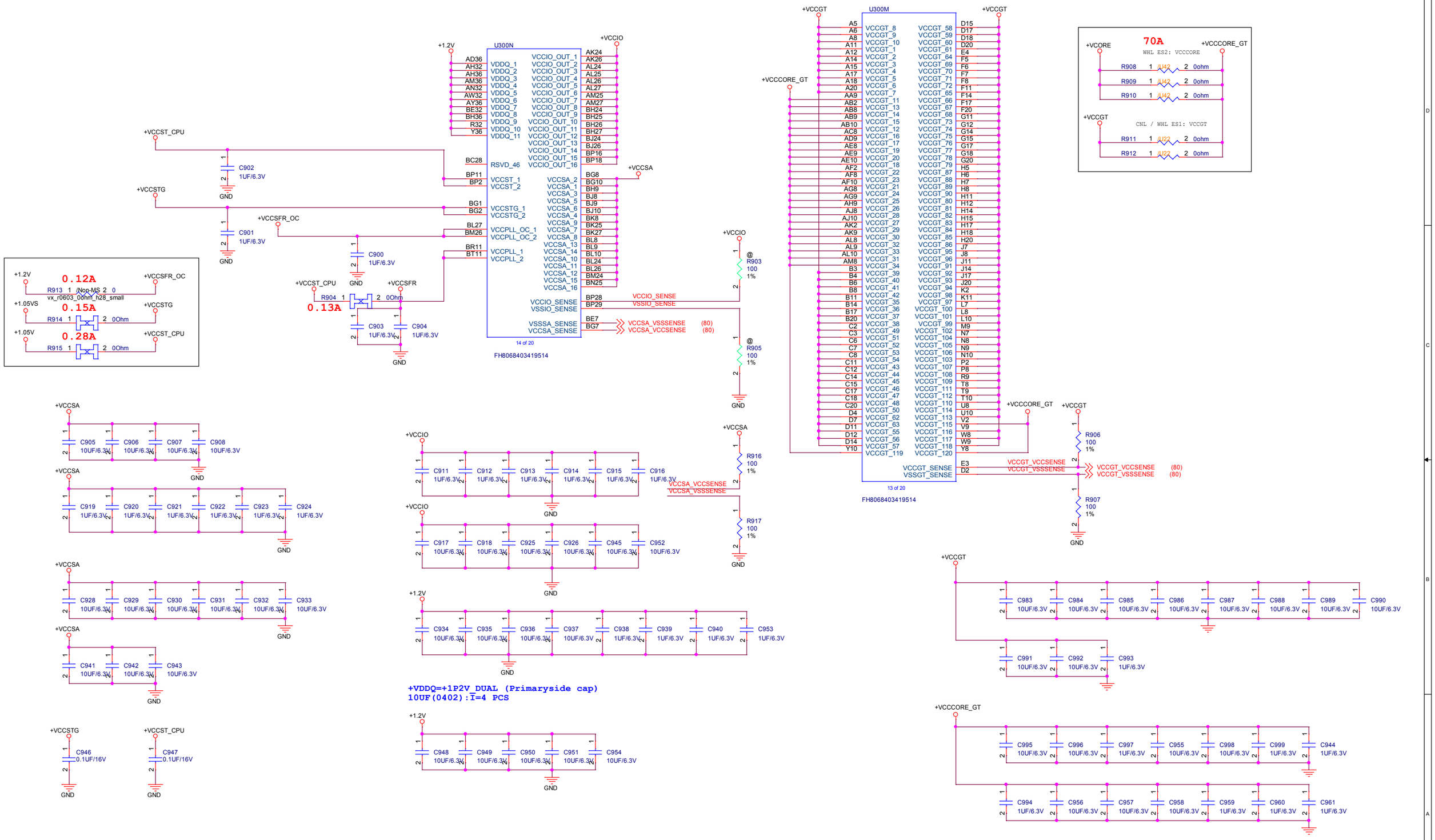
Engineer: Howard_Chen

Size	Project Name	Rev
A3	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 7 of 94



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title GPU_POWER_01
Engineer: Howard_Chen
Size Custom
Project Name MILLER
Rev 1.4
Date: Monday, June 11, 2018
Sheet 8 of 94



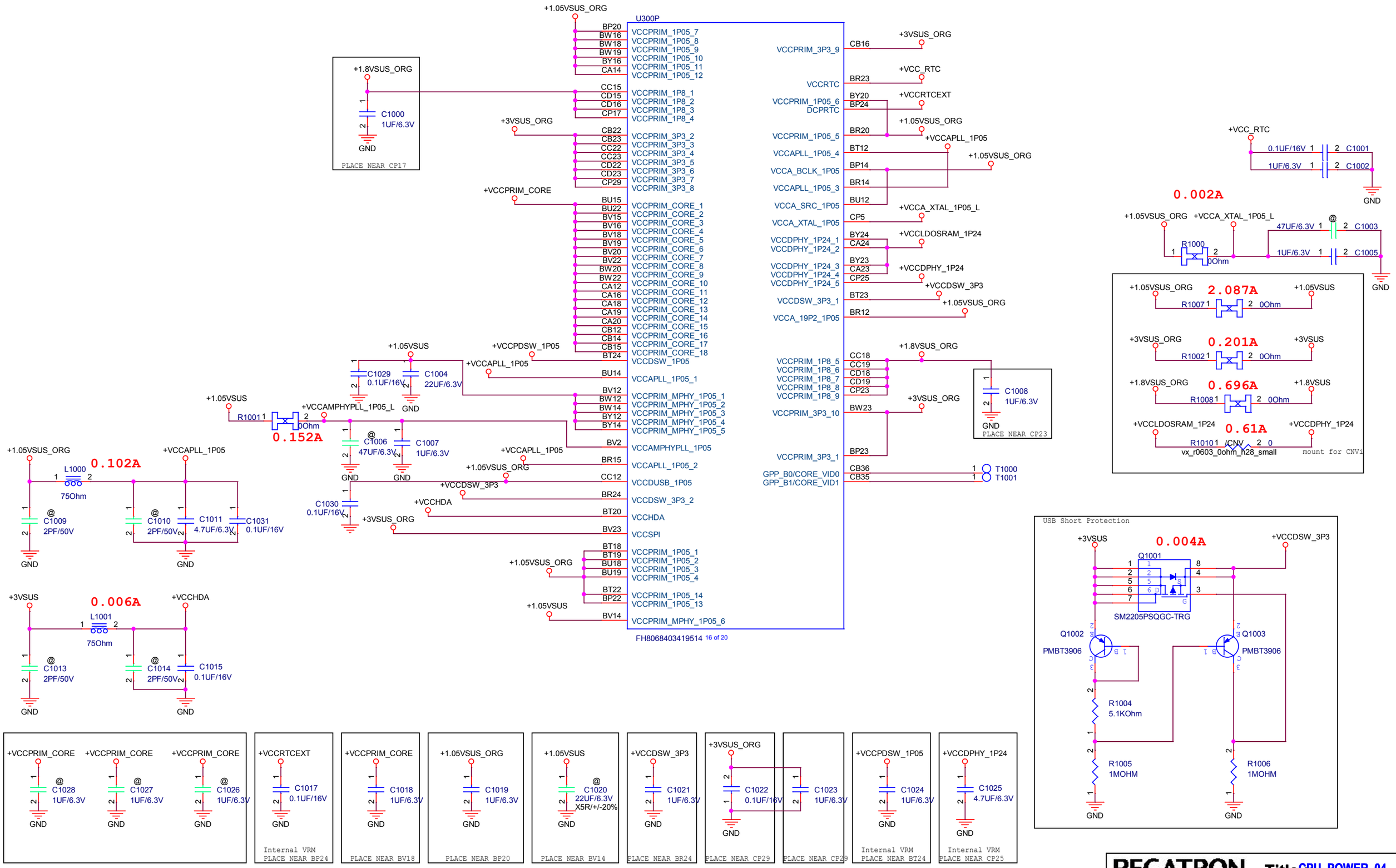
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
<OrgName>

Title: GPU_POWER_02,03

Engineer: Howard_Chen

Size: Custom | Project Name: MILLER | Rev: 1.4

Date: Monday, June 11, 2018 | Sheet 9 of 94



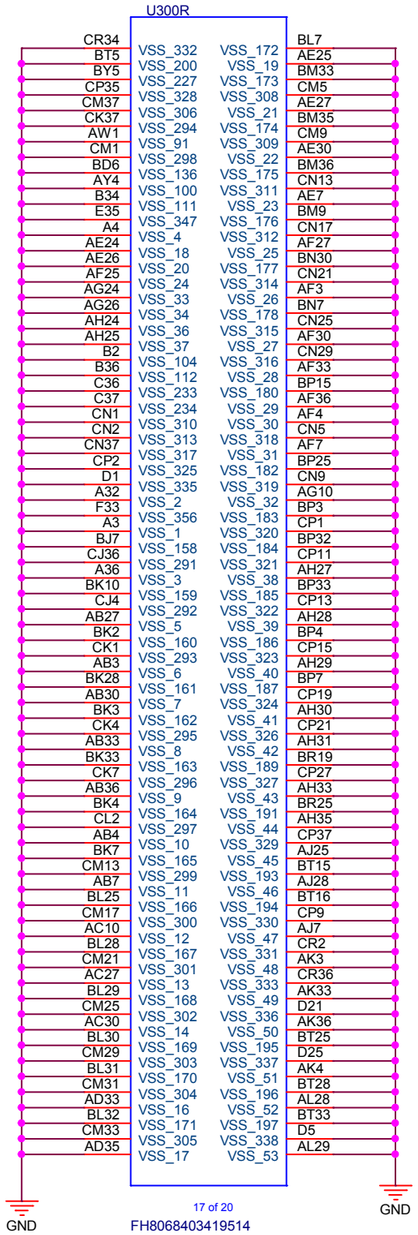
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
<OrgName>

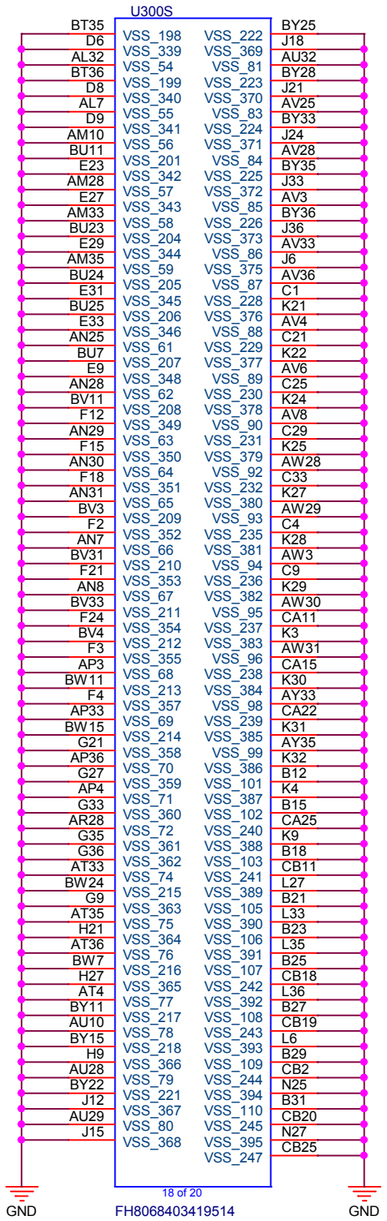
Title: CPU_POWER_04

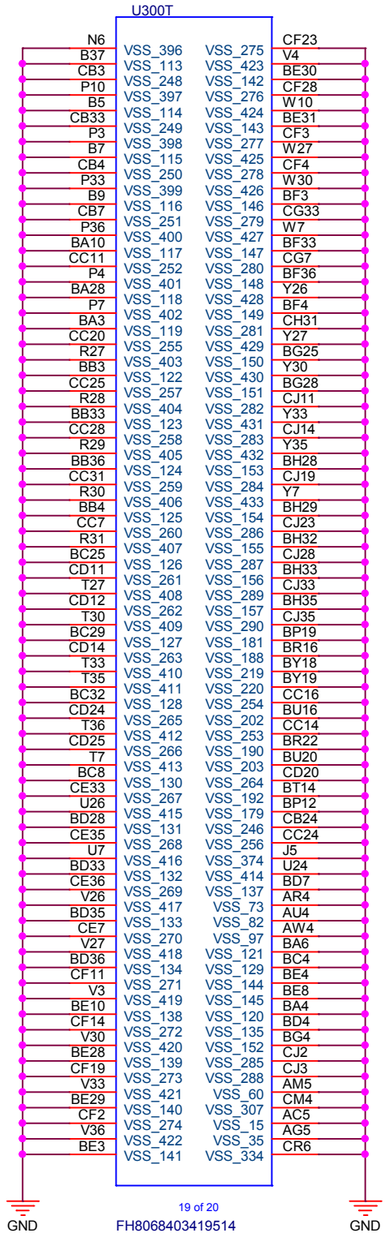
Engineer: Howard_Chen

Size	Project Name	Rev
A3	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 10 of 94







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<OrgName>

Title: CPU_GND

Engineer: Howard_Chen

Size	Project Name	Rev
A3	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 11 of 94

PEGATRON

Title : RSVD

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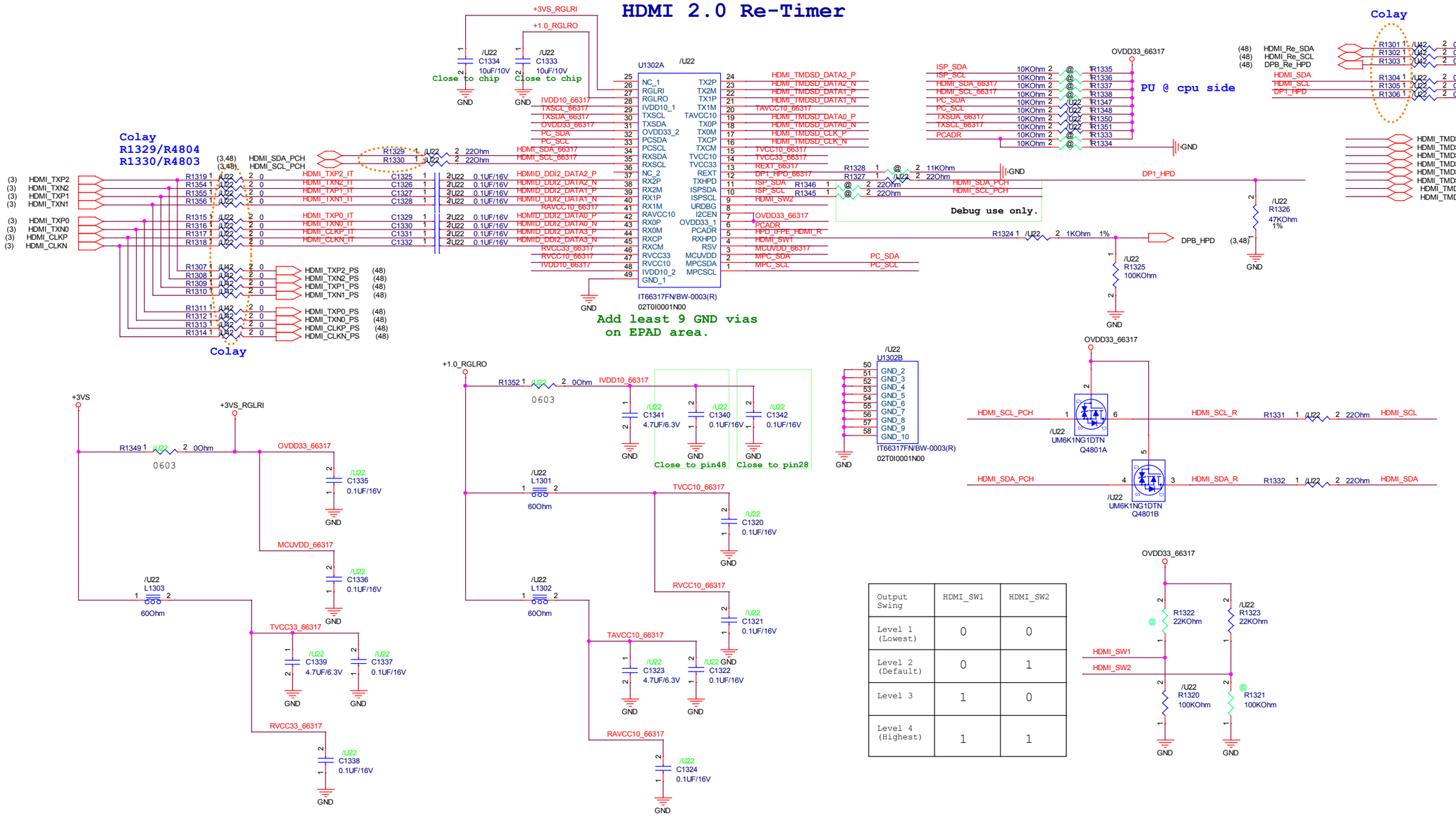
<OrgName>

Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

HDMI 2.0 Re-Timer



Output Swing	HDMI_SW1	HDMI_SW2
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

<Variant Name>

PEGATRON Title : HDMI-4K2K

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: Howard Chen

Size: Custom | Project Name: MILLER | Rev: 1.4

Date: Monday, June 11, 2018 | Sheet 13 of 94

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

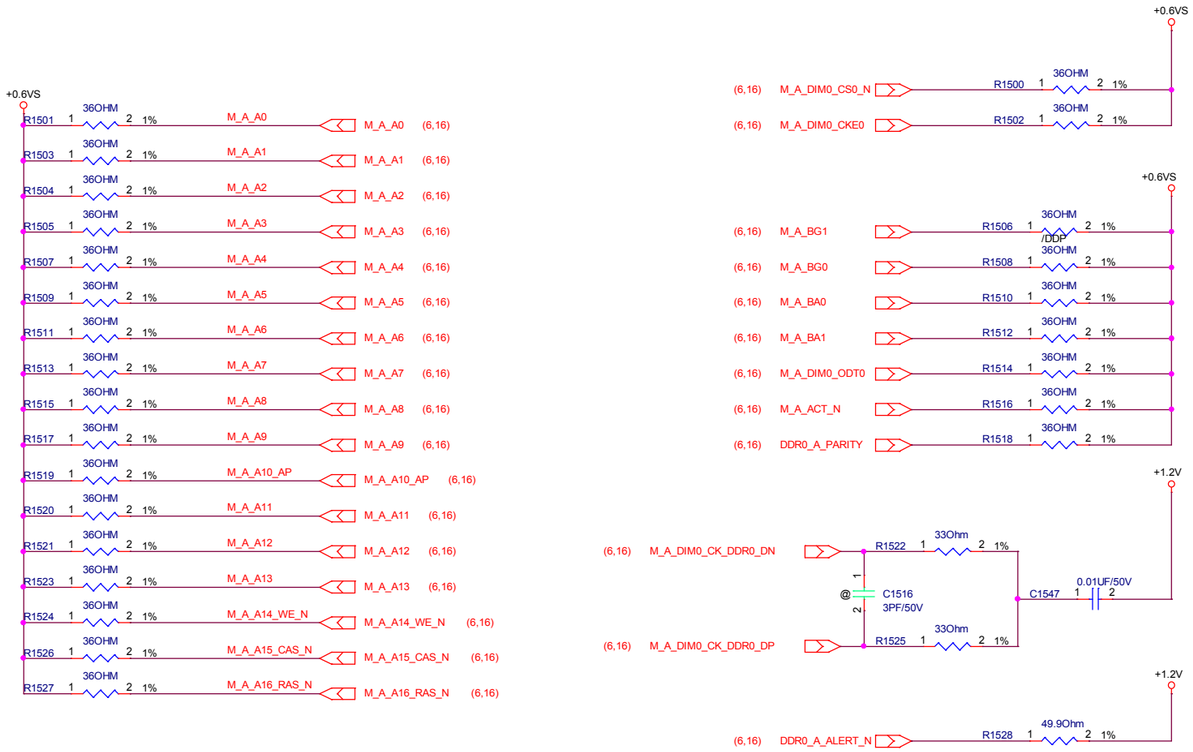
Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

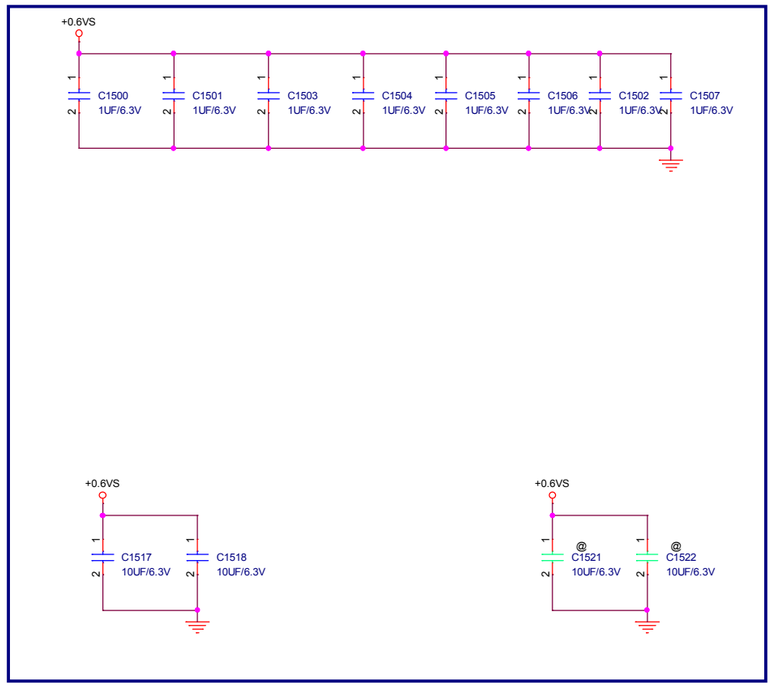
15 DDR4(0)_Termination

CHA

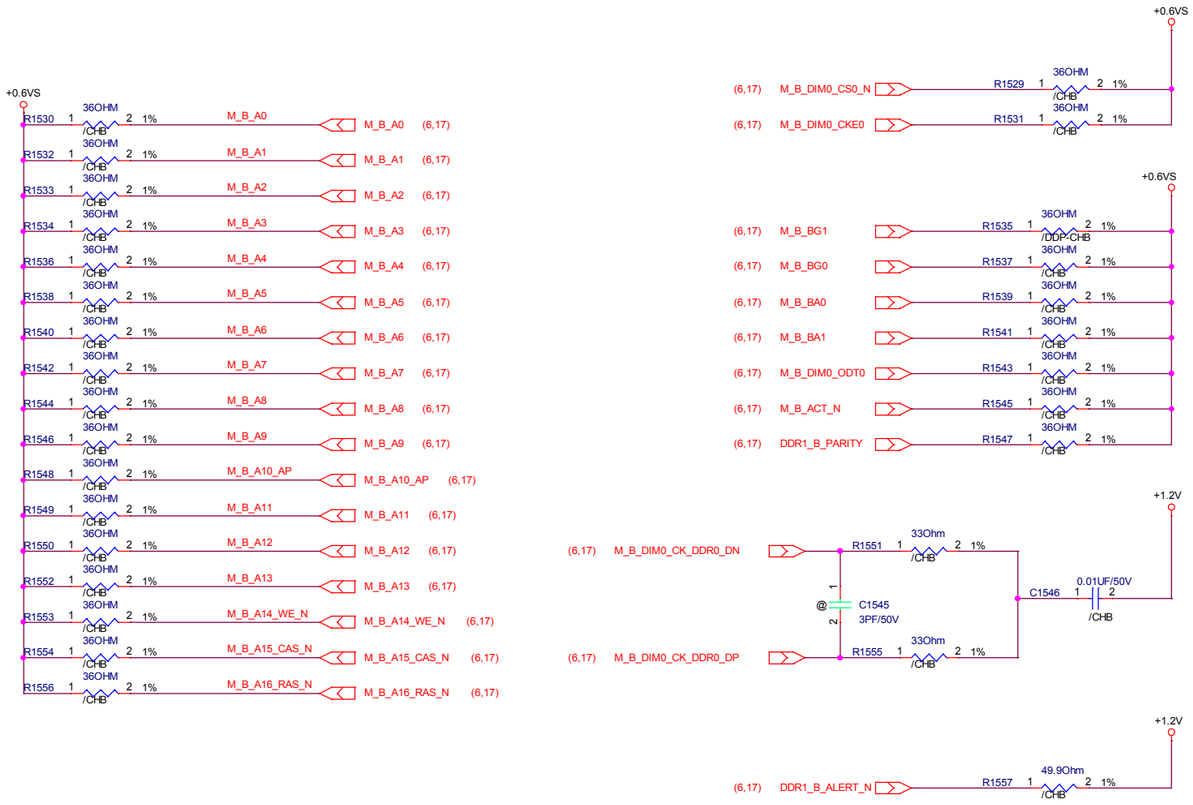


Average placed close to +VDDQ_VTT power plane

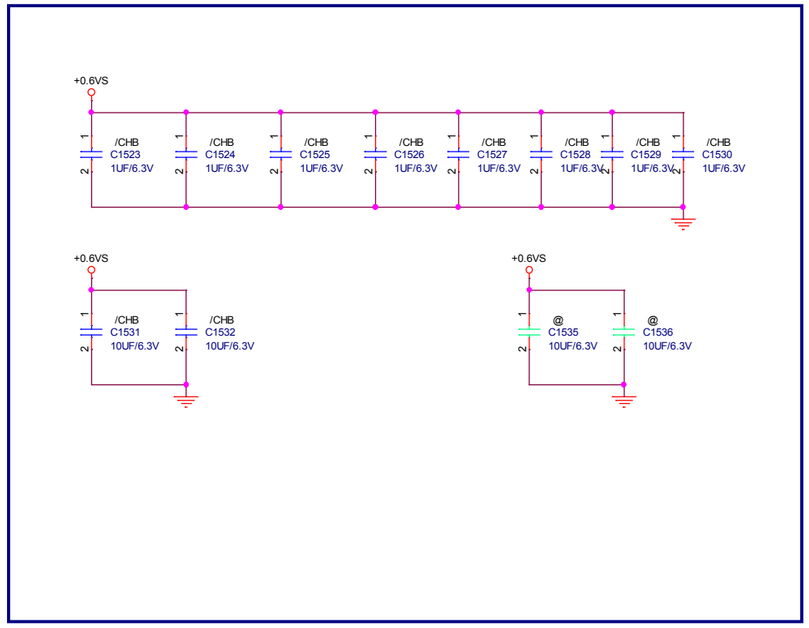
Follow intel PDG #575412 0.7



CHB



Follow intel PDG #575412 0.7



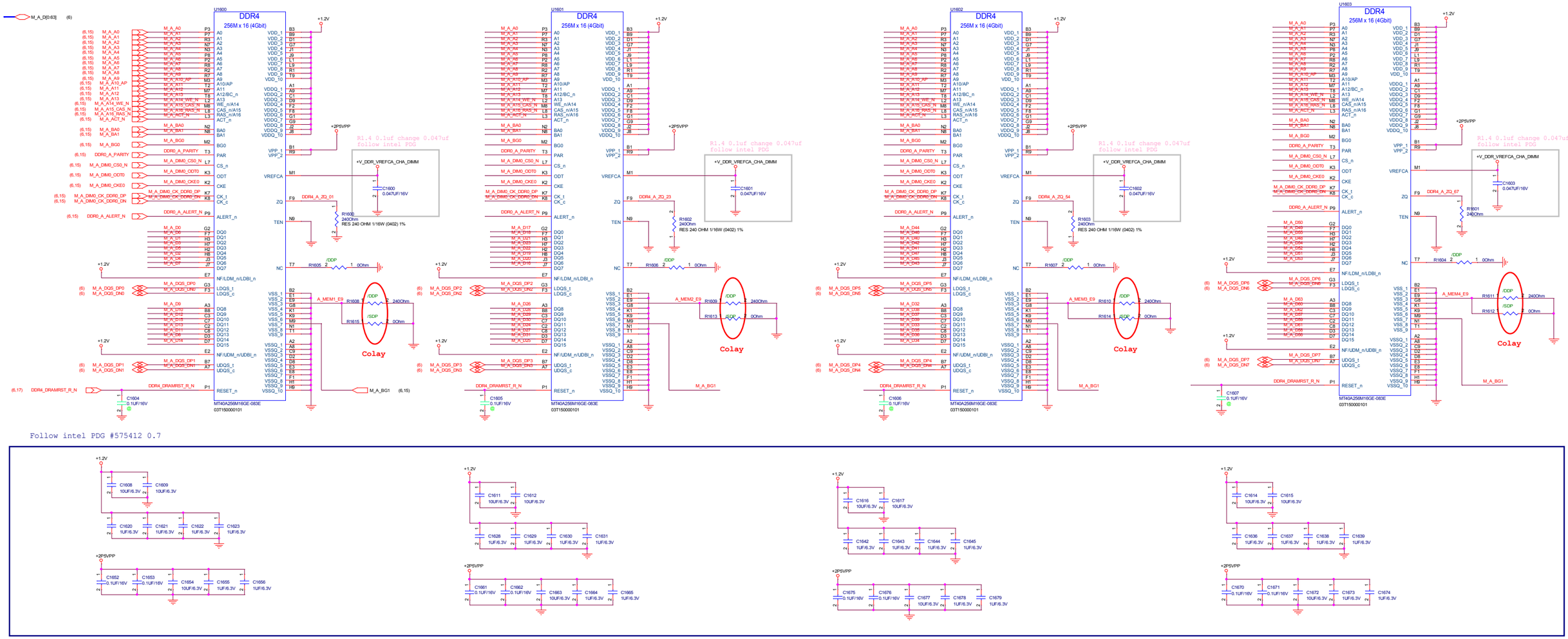
PEGATRON Title : DDR4(0)_Termination

BG1-HW3 RD Engineer: Howard Chen

Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 15 of 94

16 DDR4(1)_CH0



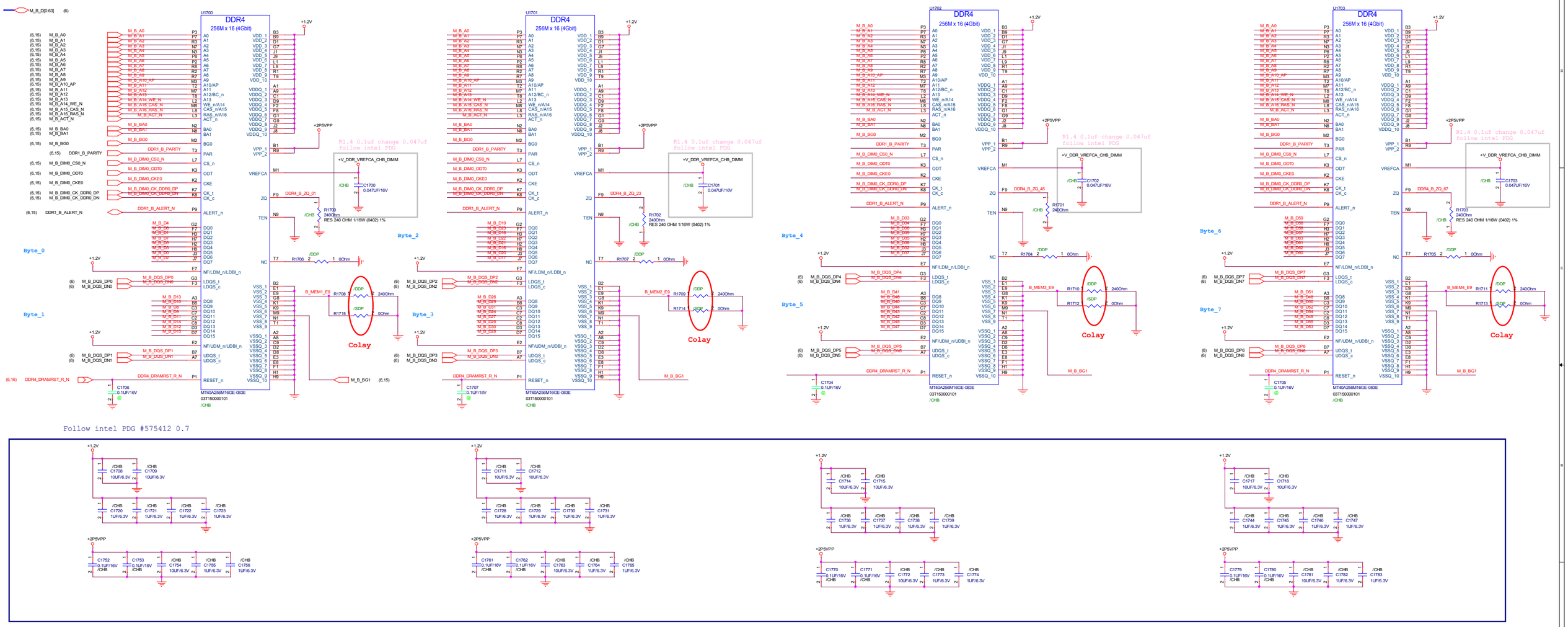
PEGATRON Title : DDR4(1) CH0

BG1-HW3 RD Engineer: Howard Chen

Size	Project Name	Rev
Custom	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 16 of 94

17 DDR4(2)_CH1



Follow intel PDG #575412 0.7

PEGATRON Title : DDR4(2)_CH1

BG1-HW3 RD Engineer: Howard Chen

Size	Project Name	Rev
Custom	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 17 of 94

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

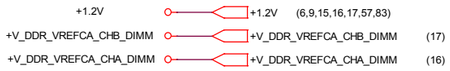
<OrgName>

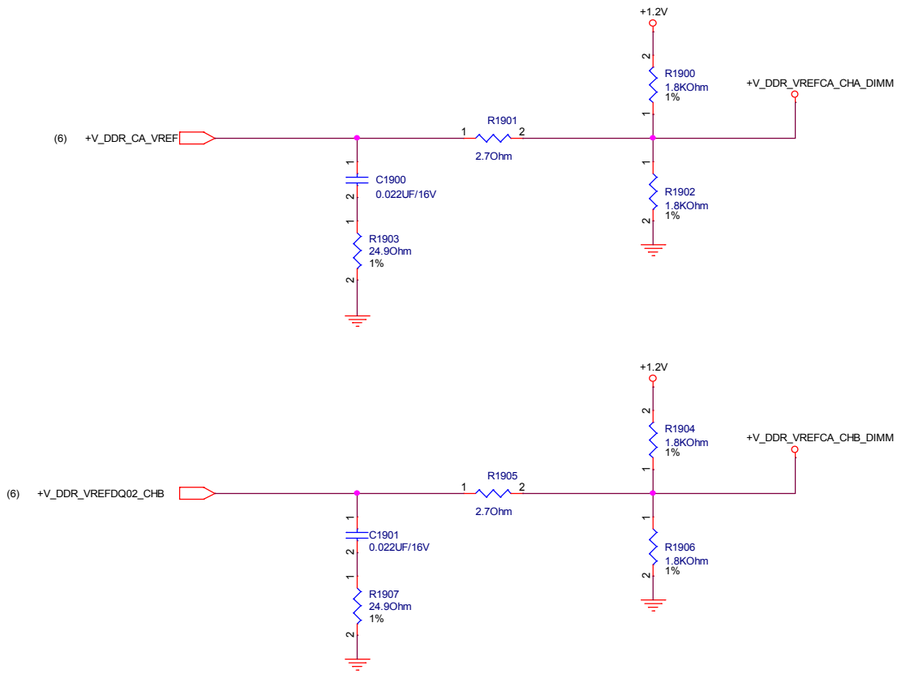
Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

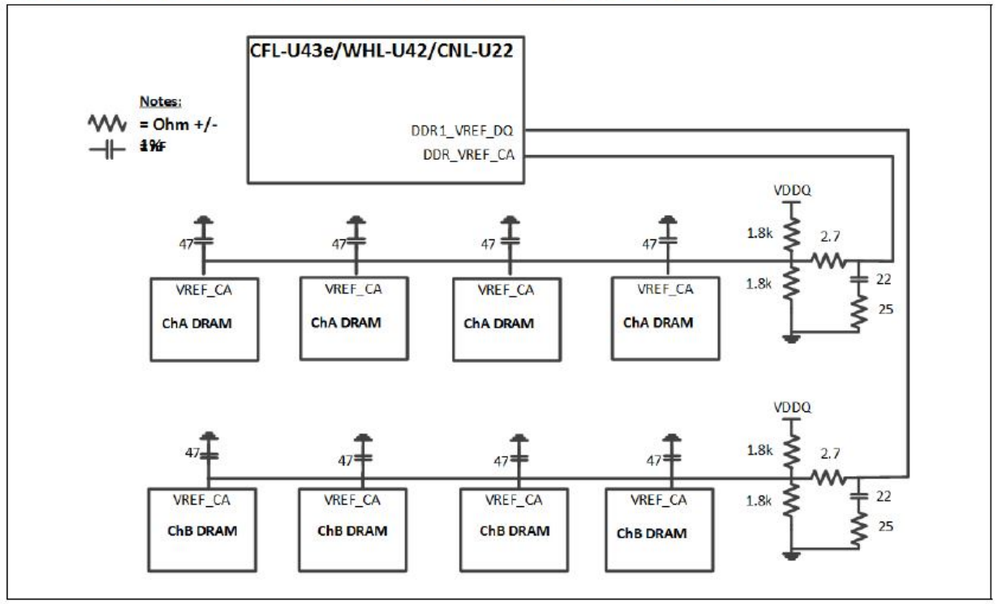
Date: Monday, June 11, 2018

19 DDR4(3)_CA/DQ Voltage



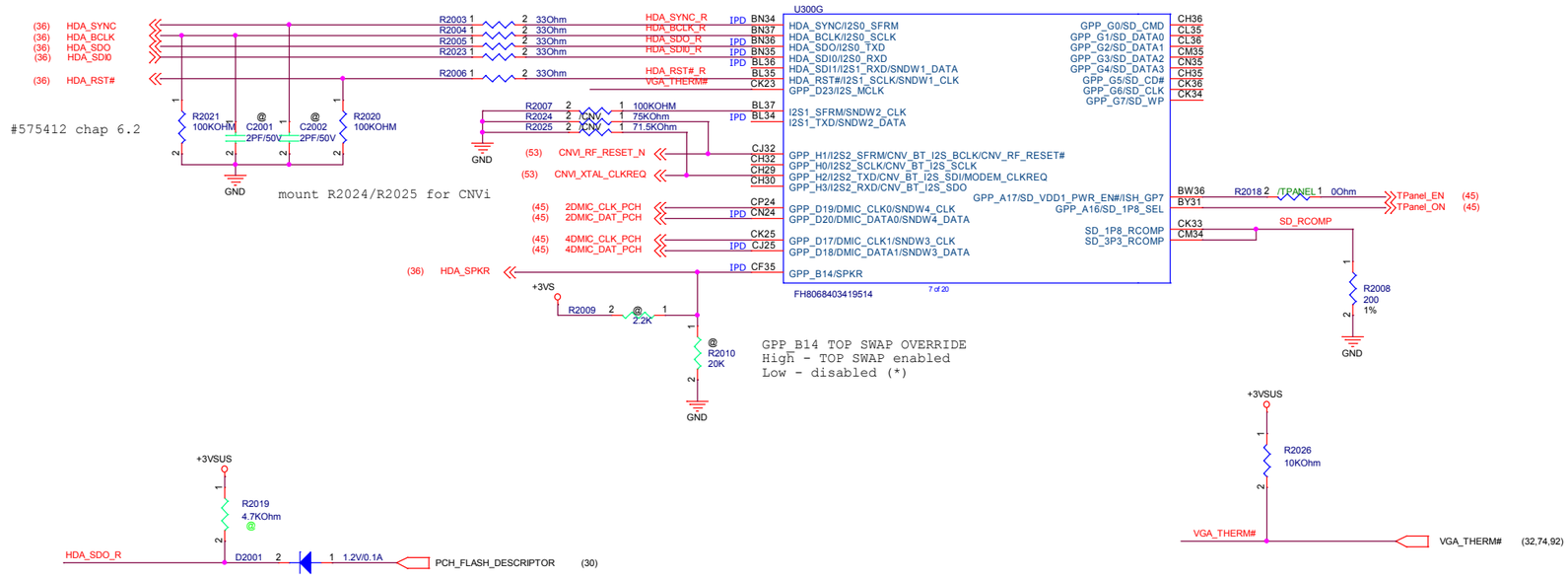


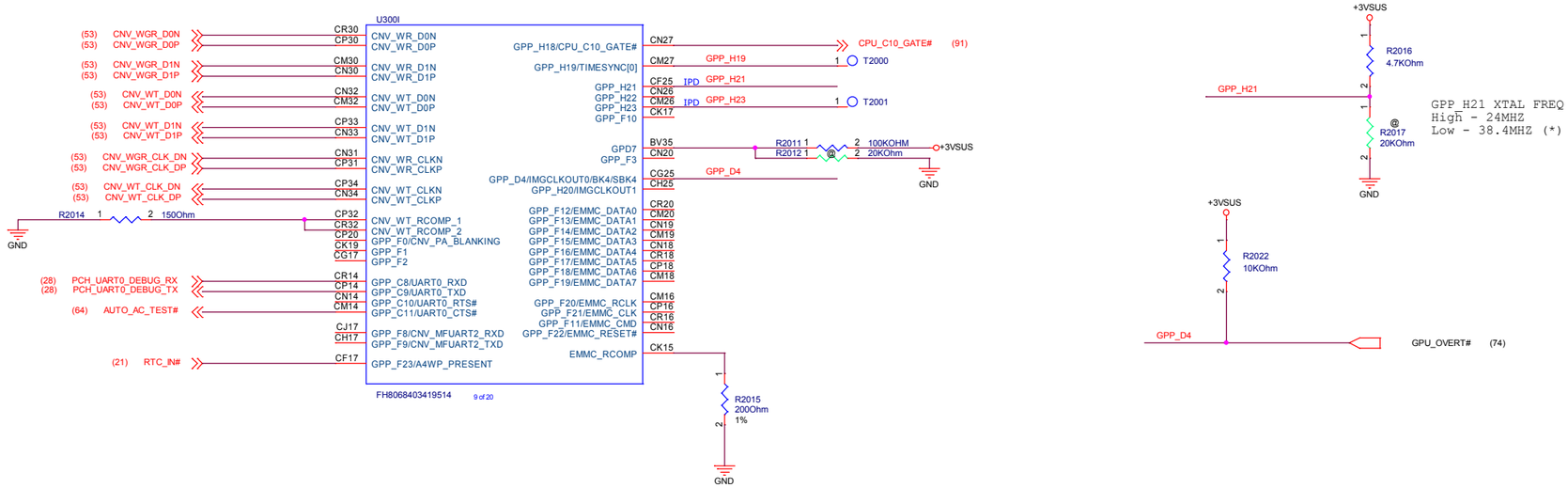
WHL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview



PEGATRON	Title : DDR4(3)_CA/DQ Voltage		
BG1/HW1	Engineer: Howard Chen		
Size C	Project Name MILLER		Rev 1.4
Date: Monday, June 11, 2018	Sheet 19 of 94		

HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "top swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling





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Title: PCH_AUDIO,SDIO,CSI2
Engineer: Howard Chen
Size: A2
Project Name: MILLER
Rev: 1.4
Date: Monday, June 11, 2018
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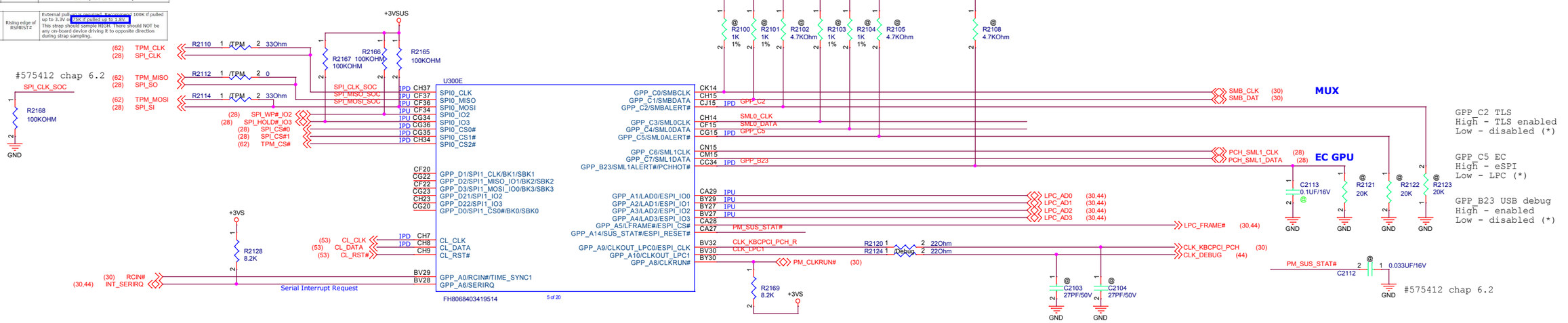
GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. **0 = Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) **1 = Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. **0 = LPC** is selected (for EC). (Default) **1 = eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

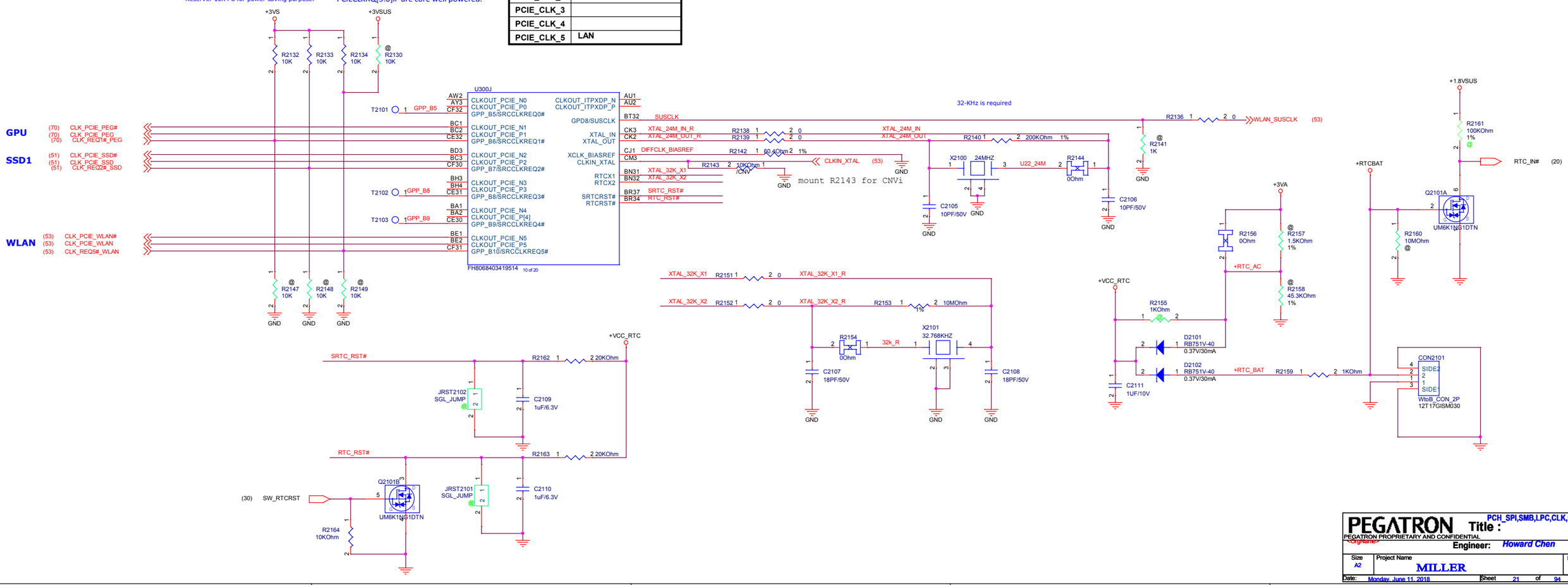
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. **0 = Disable** Intel® DCI-OOB (Default) **1 = Enable** Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

PCH CLKREQ Setting:
Not connected to device.
PCIECLKRQ[5:0]# are core well powered.

PCIE_CLK_0	
PCIE_CLK_1	GPU
PCIE_CLK_2	SSD
PCIE_CLK_3	
PCIE_CLK_4	
PCIE_CLK_5	LAN



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PCH_SPI,SMB,LPC,CLK,RTC
Engineer: Howard Chen

Size	Project Name	Rev
A2	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 21 of 94

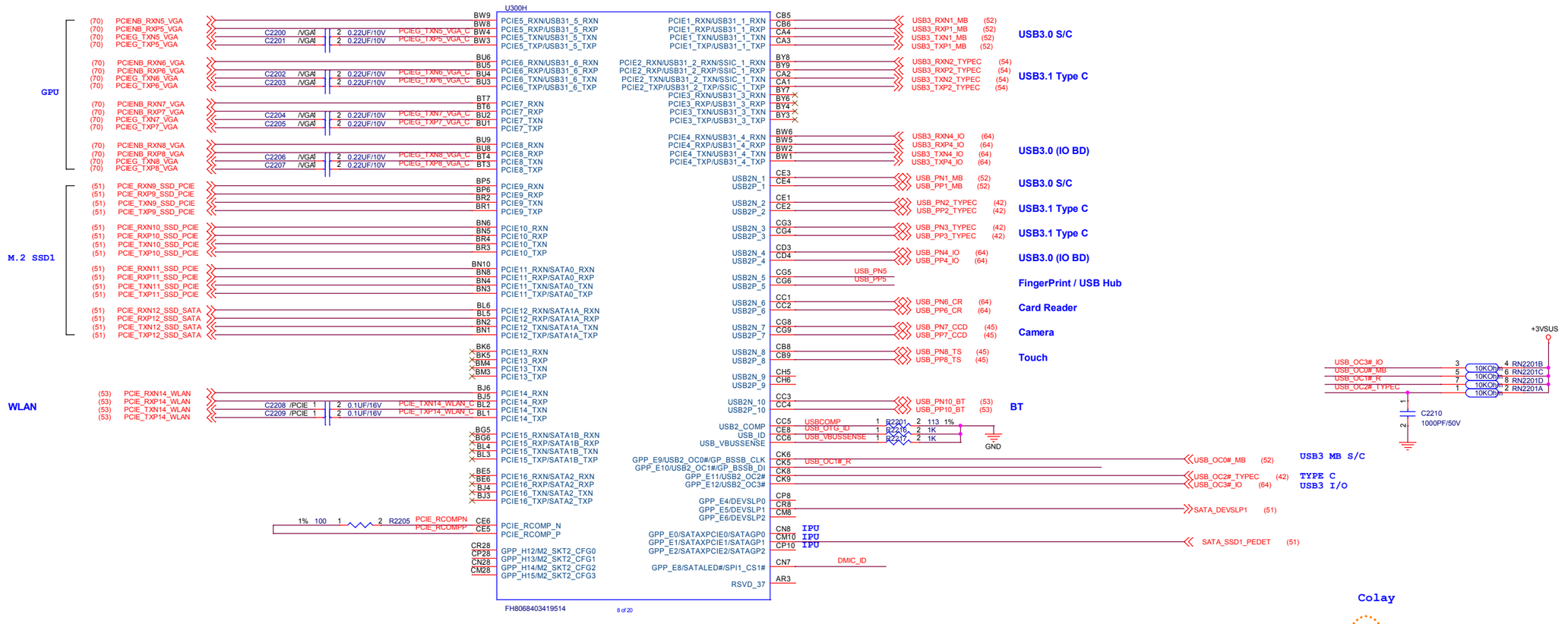
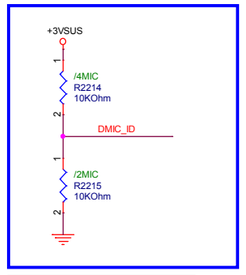


Table 1-3. PCH HSIO Detail

SKU	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Mainstream/ Base-U	USB3.1 Gen1/ Gen2	USB3.1 Gen1/ Gen2	USB3.1 Gen1/ Gen2	USB3.1 Gen1/ Gen2	PCIe*/ USB3.1 Gen1/ Gen2	PCIe*/ USB3.1 Gen1/ Gen2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0A	PCIe*/ SATA 1A	PCIe*/ GbE 0D	GbE 0E/ PCIe*	PCIe*	PCIe*
Premium-U	PCIe*/ USB3.1 Gen1/ Gen2	PCIe*/ USB3.1 Gen1/ Gen2	PCIe*/ USB3.1 Gen1/ Gen2	PCIe*/ USB3.1 Gen1/ Gen2	PCIe*/ USB3.1 Gen1/ Gen2	PCIe*/ USB3.1 Gen1/ Gen2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0A	PCIe*/ SATA 1A	GbE 0D/ PCIe*	GbE 0E/ PCIe*	PCIe*	PCIe*/ SATA 2

DMIC ID



	DMIC ID
4 DMIC	1
2 DMIC	0

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: PCH_PCIE,USB,SATA
Engineer: Howard Chen
Size: A2
Project Name: MILLER
Rev: 1.4
Date: Monday, June 11, 2018
Sheet 22 of 94

GPP_B18 No Reboot
High - enabled
Low - disabled (*)

GPP_B22 Boot ROM
High - LPC
Low - SPI (*)

GPP_F6 Intergrated CNVi
High - disabled
Low - enabled

#575412 chap 6.2

U300F

FH8068403419514 6 of 20

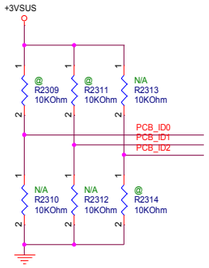
GPP_D12 JTAG ODT
High - enabled
Low - disabled

6/30
CNVi Intel recommand unmount R2306
7/3
Intel's feedback:
JFP has internal PD,
so don't need to put an external resistor.

mount R2302/R2304 for CNVi

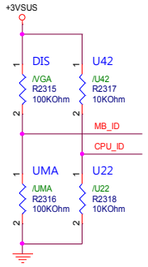
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit 88fs	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). Bit 6 Boot BIOS Destination 0 SPI (Default) 1 LPC. Notes: 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash (connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Strapping GPP_B22 to select LPC, or using the functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 10K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enabled. 1 = Integrated CNVi disabled.

PCB ID



	PCB_ID2 (GPP_C15)	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R10	0	0	0
R11	0	0	1
R12	0	1	0
R13	0	1	1
R14	1	0	0
R15	1	0	1
R20	1	1	0

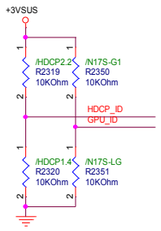
CPU BD ID



	CPU_ID
CNL U22	0
WHL U42	1

	MB_ID
UMA	0
DIS	1

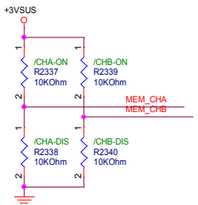
HDCP ID
GPU ID



	HDCP_ID
HDCP 1.4	0
HDCP 2.2	1

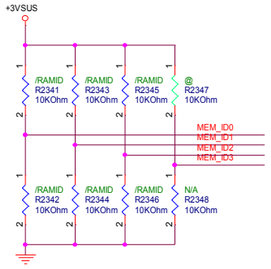
	GPU_ID
N17S-LG	0
N17S-G1	1

MEM TEST ID



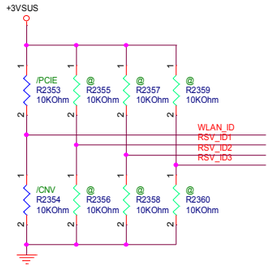
	CHA	CHB
Disable	0	
Enable	1	
Disable		0
Enable		1

MEM ID



	MEM_ID3 (GPP_A21)	MEM_ID2 (GPP_A20)	MEM_ID1 (GPP_A19)	MEM_ID0 (GPP_A18)
MICRON MT40A512M16LY-075:E SDP 0315-02DW0PB	0	0	0	0
HYNIX H5AN8G6NCJR-VKC SDP 0315-02GJ0PB	0	0	0	1
HYNIX H5AN8G6NAFR-UHC SDP 0315-01W60PB	0	0	1	0
HYNIX H5ANAG6NAMR-UHC DDP 0315-02640PB	0	0	1	1
MICRON MT40A1G16WBU-083E:B DDP 0315-01YC0PB	0	1	0	0
MICRON MT40A1G16KNR-075:E DDP 0315-02FY0PB	0	1	0	1
	0	1	1	0

WLAN ID



	WLAN_ID
CNVI	0
PCIE	1

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: PCH_GPIO
Engineer: Howard Chen
Size: Custom
Project Name: MILLER
Rev: 1.4
Date: Monday, June 11, 2018
Sheet 23 of 94

PEGATRON Title :RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1

Engineer: *Howard Chen*

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 24 of 94

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1

Engineer: *Howard Chen*

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 25 of 94

PEGATRON Title :RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1

Engineer: *Howard Chen*

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 26 of 94

PEGATRON

Title : RSVD

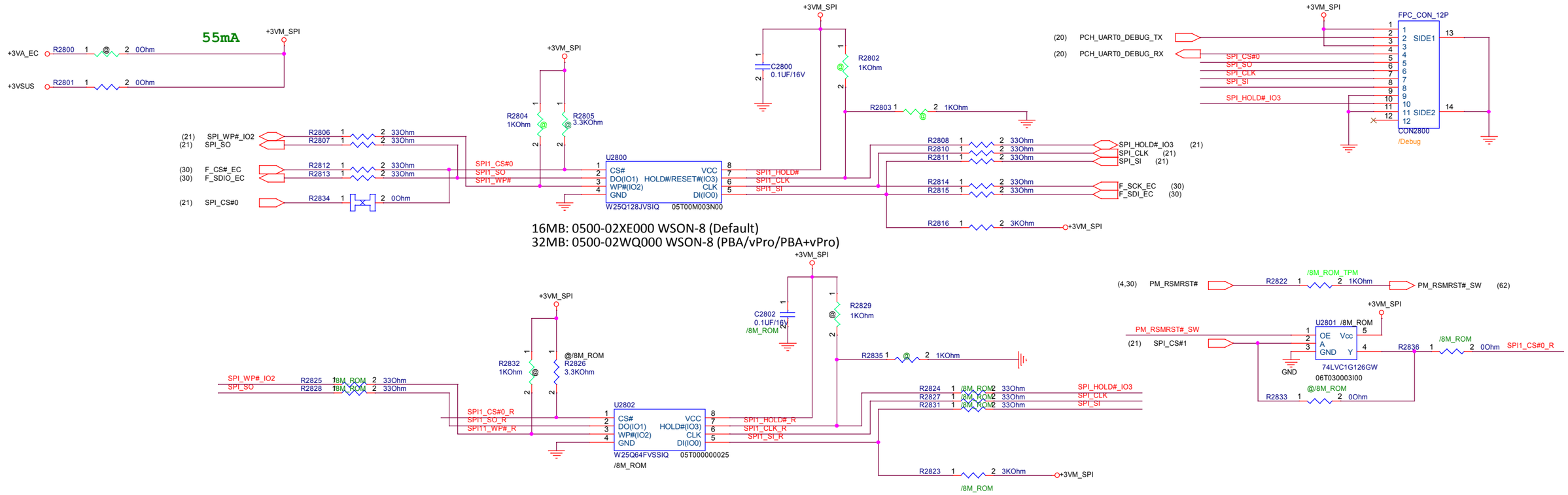
PEGATRON PROPRIETARY AND CONFIDENTIAL

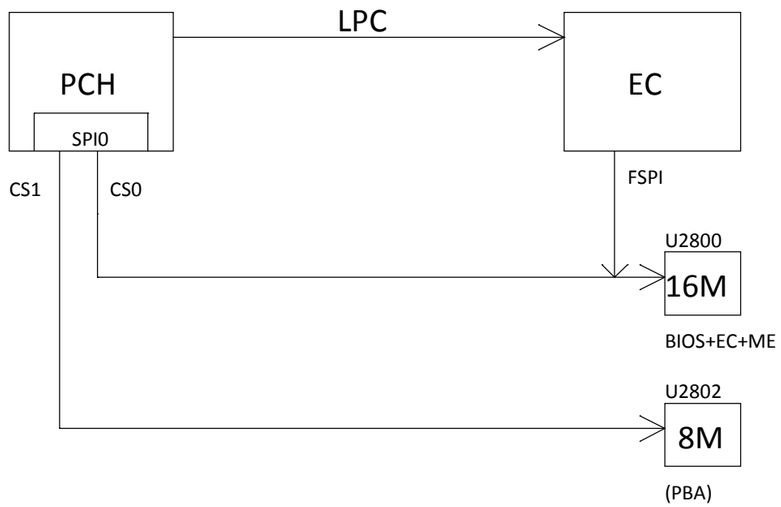
<OrgName>

Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

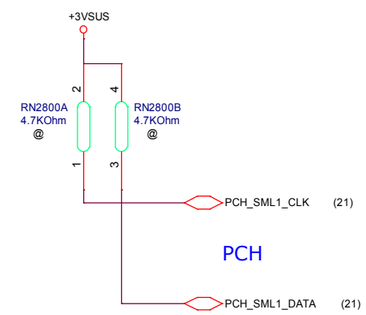




EC

GPU

PCH SMBus



PEGATRON Title : PCH(9)_SPI_SMB

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1 Engineer: Howard Chen

Size	Project Name	Rev
Custom	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 28 of 94

PEGATRON

Title : RSVD

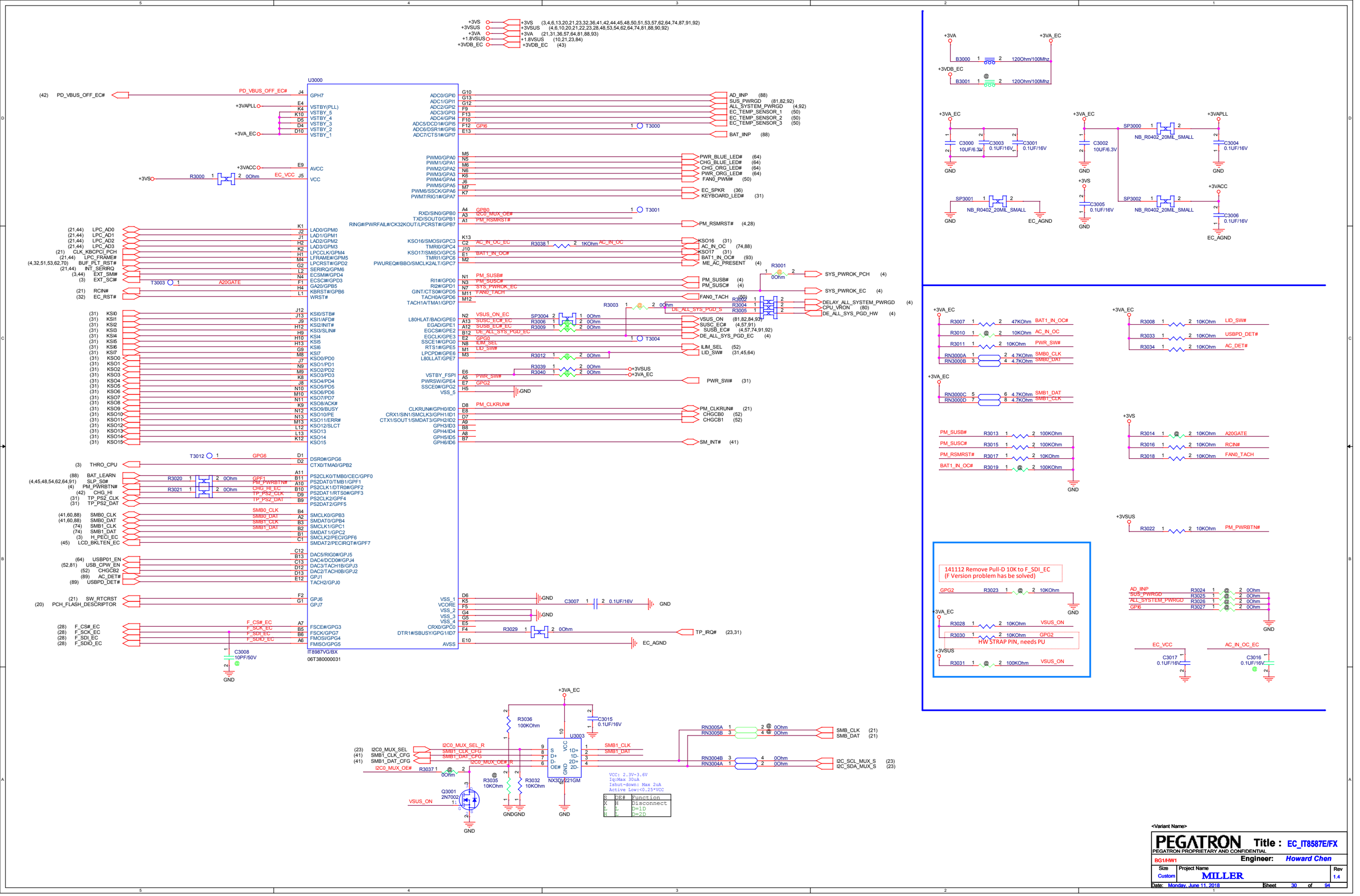
PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018



<Variant Name>

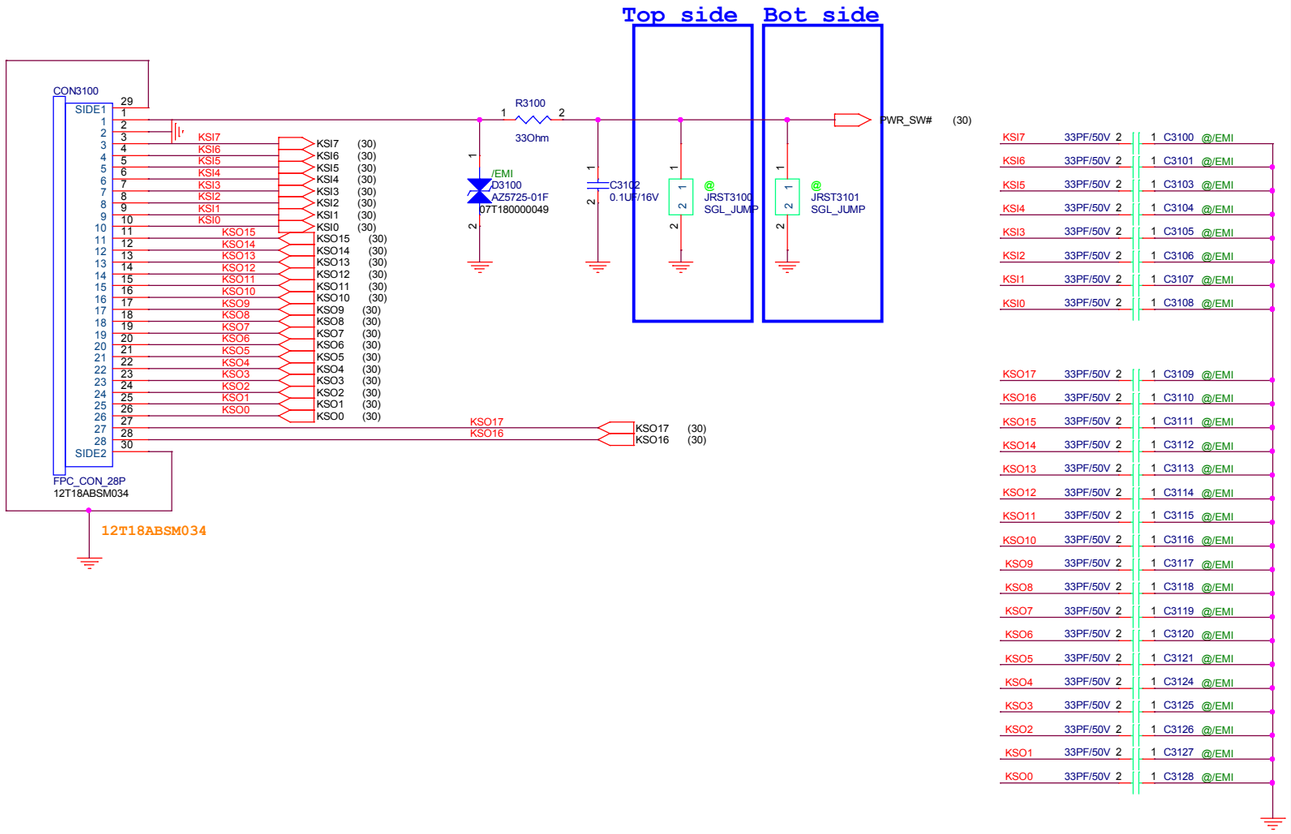
PEGATRON Title : EC_IT8587E/FX

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1 Engineer: Howard Chen

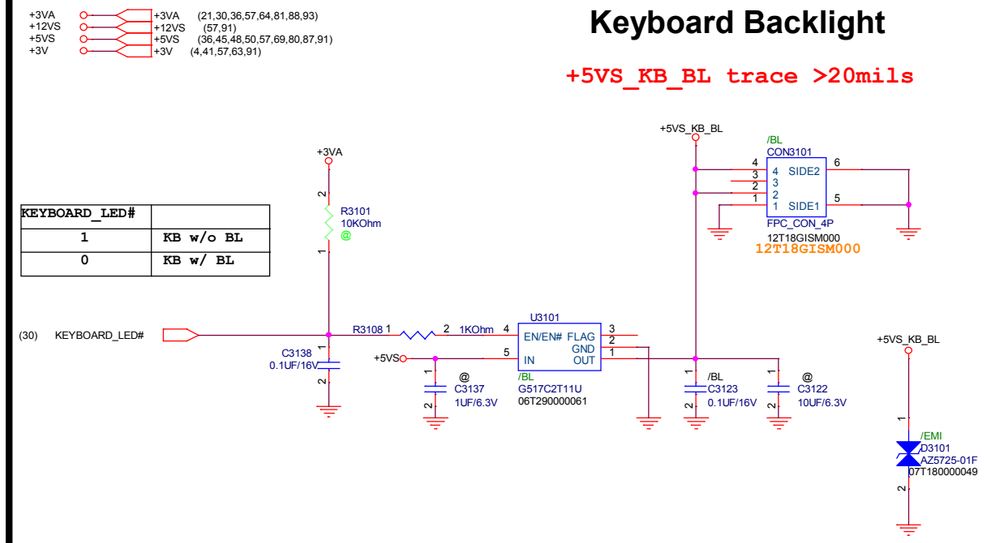
Size	Project Name	Rev
Custom	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 30 of 94



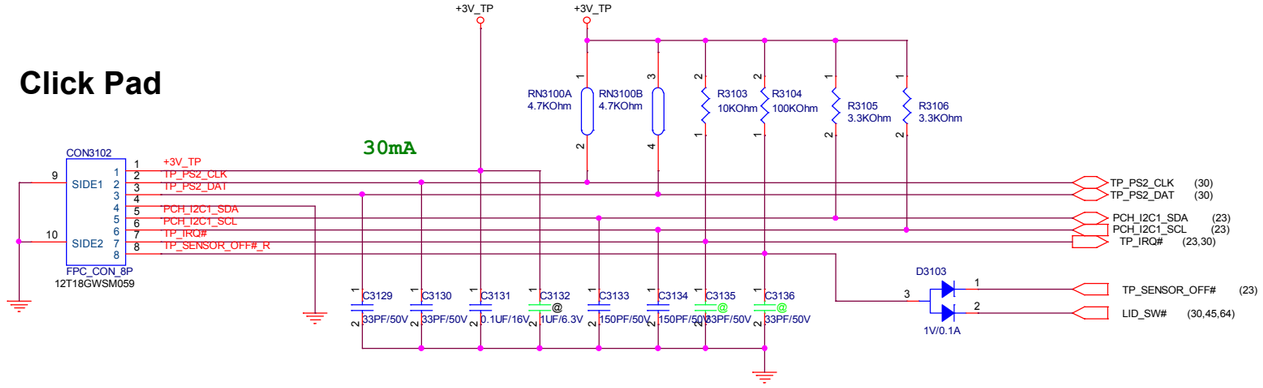
Keyboard Backlight

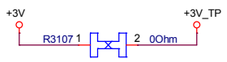
+5VS_KB_BL trace >20mils

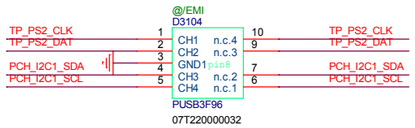


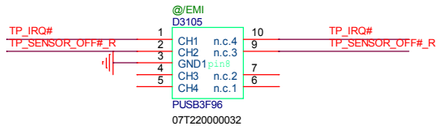
KEYBOARD_LED#	
1	KB w/o BL
0	KB w/ BL

Click Pad

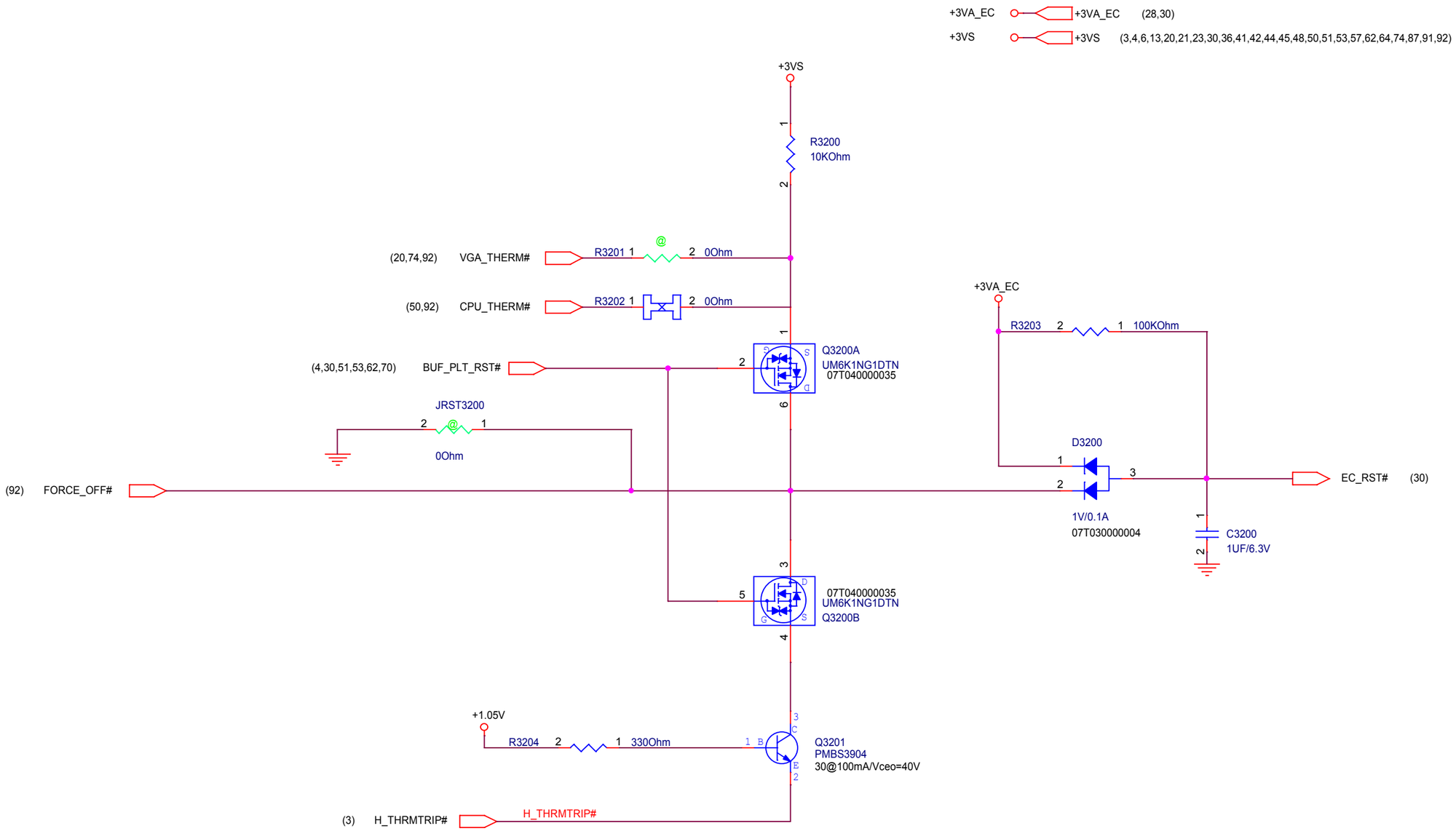








PEGATRON	Title : KB_TP		
BG1/HW1	Engineer: Howard Chen		
Size C	Project Name MILLER		Rev 1.4
Date: Monday, June 11, 2018	Sheet 31 of 94		



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST_Reset Circuit

BG1/HW1

Engineer: Howard Chen

Size	Project Name	Rev
B	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 32 of 94

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

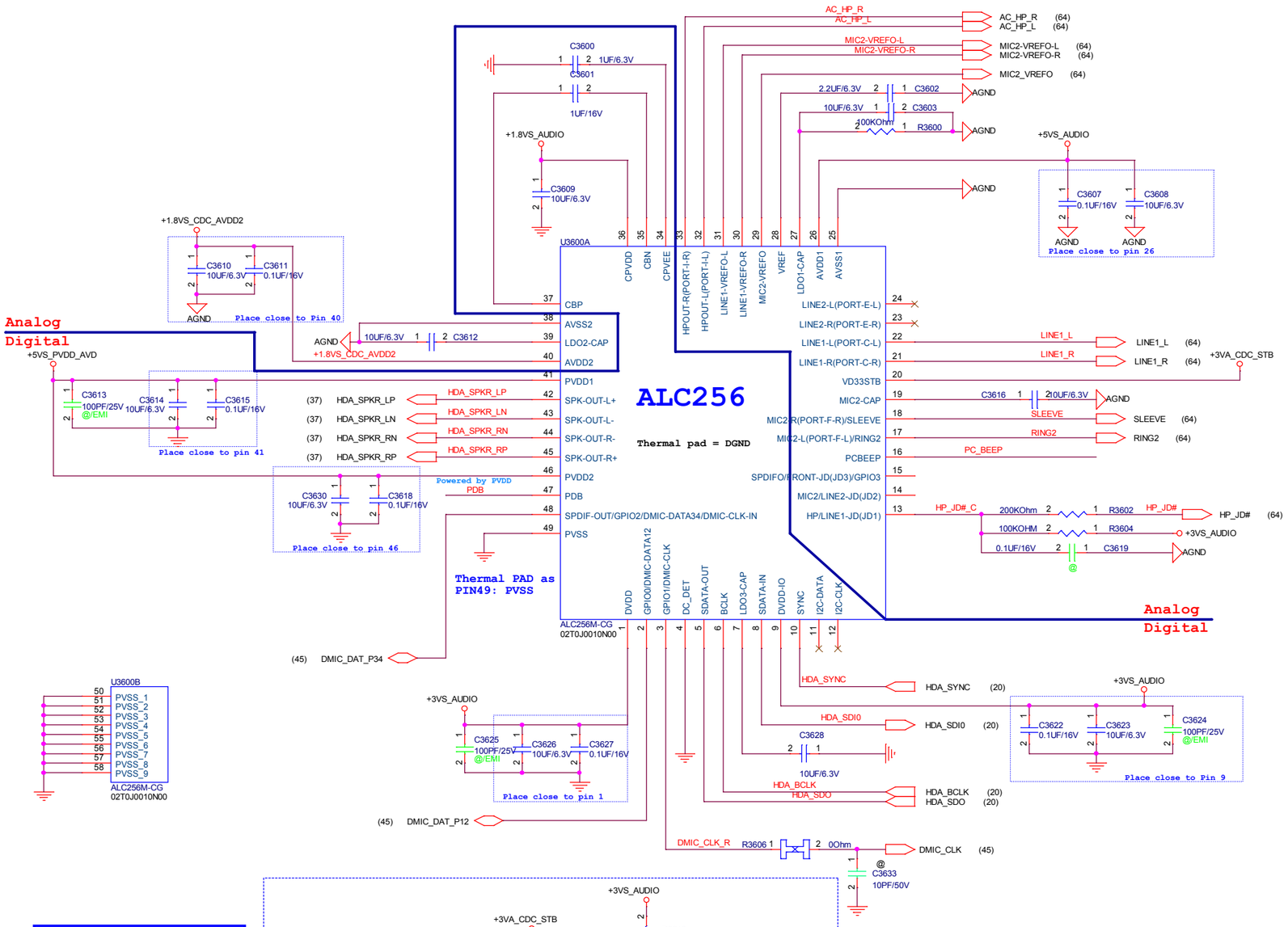
<OrgName>

Engineer: *Howard Chen*

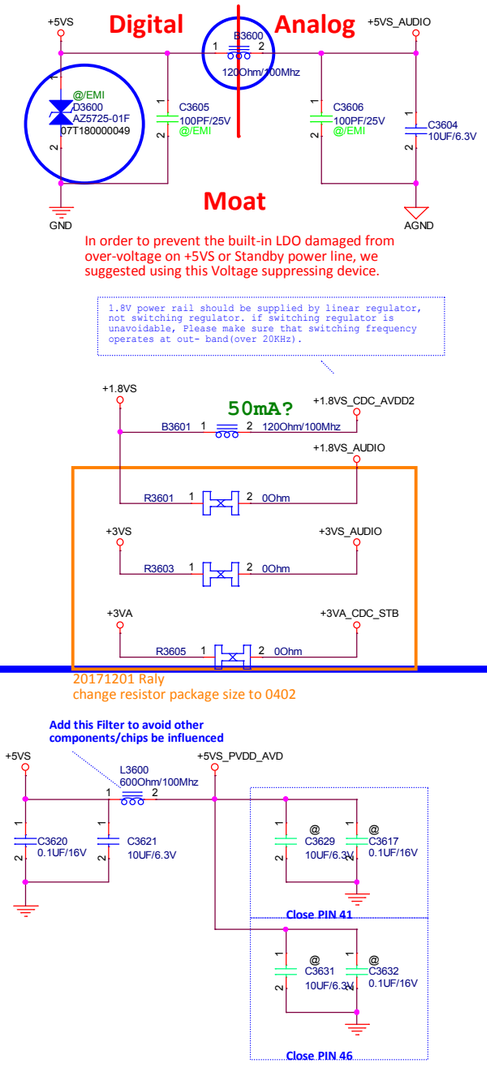
Size	Project Name	Rev
A	MILLER	1.4

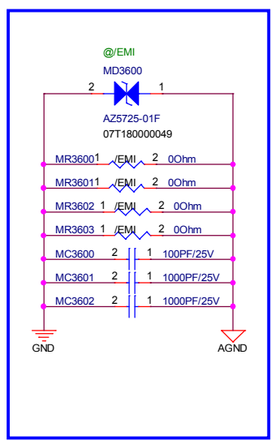
Date: Monday, June 11, 2018

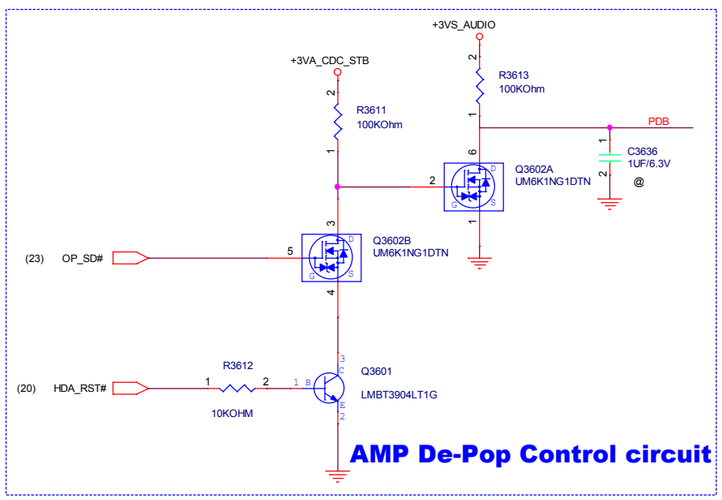
Audio Codec



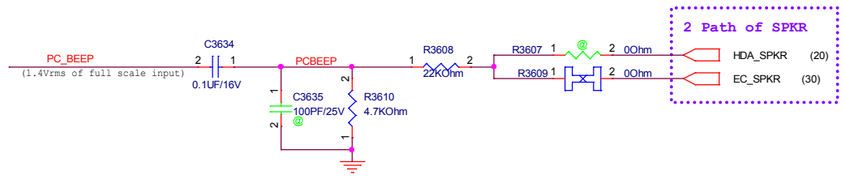
Codec Power







PC BEEP



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW1

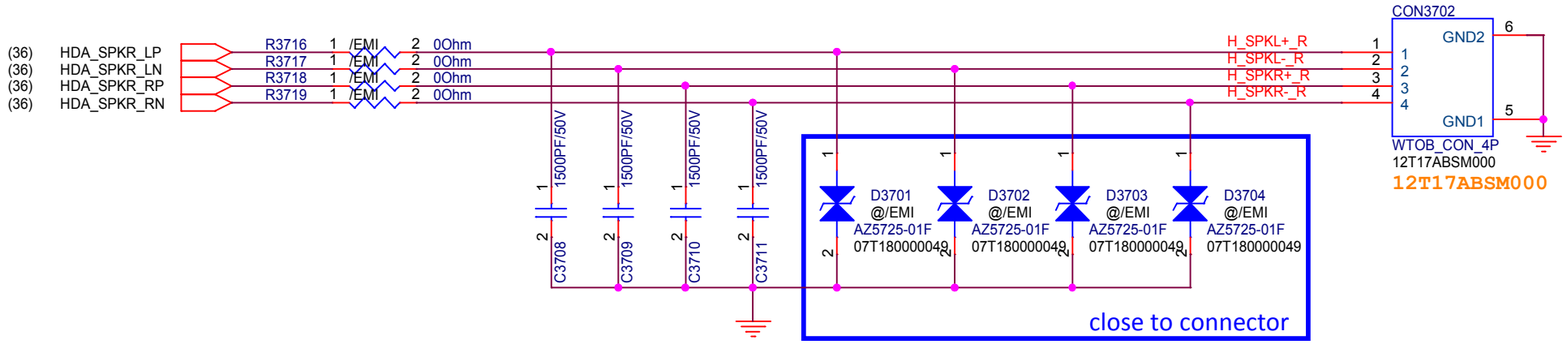
Title : Audio Codec ALC256

Engineer: Howard Chen

Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 36 of 94

Internal Speaker



PEGATRON Title : AUD_HP/DMIC/SPK

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD

Engineer: *Howard Chen*

Size	Project Name	Rev
B	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 37 of 94

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: *Howard Chen*

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: *Howard Chen*

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

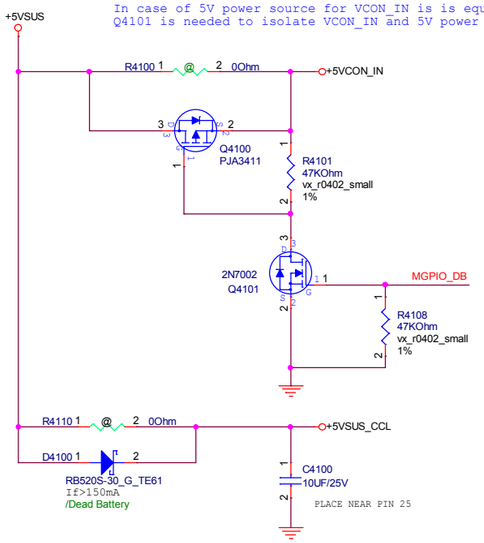
<OrgName>

Engineer: Howard Chen

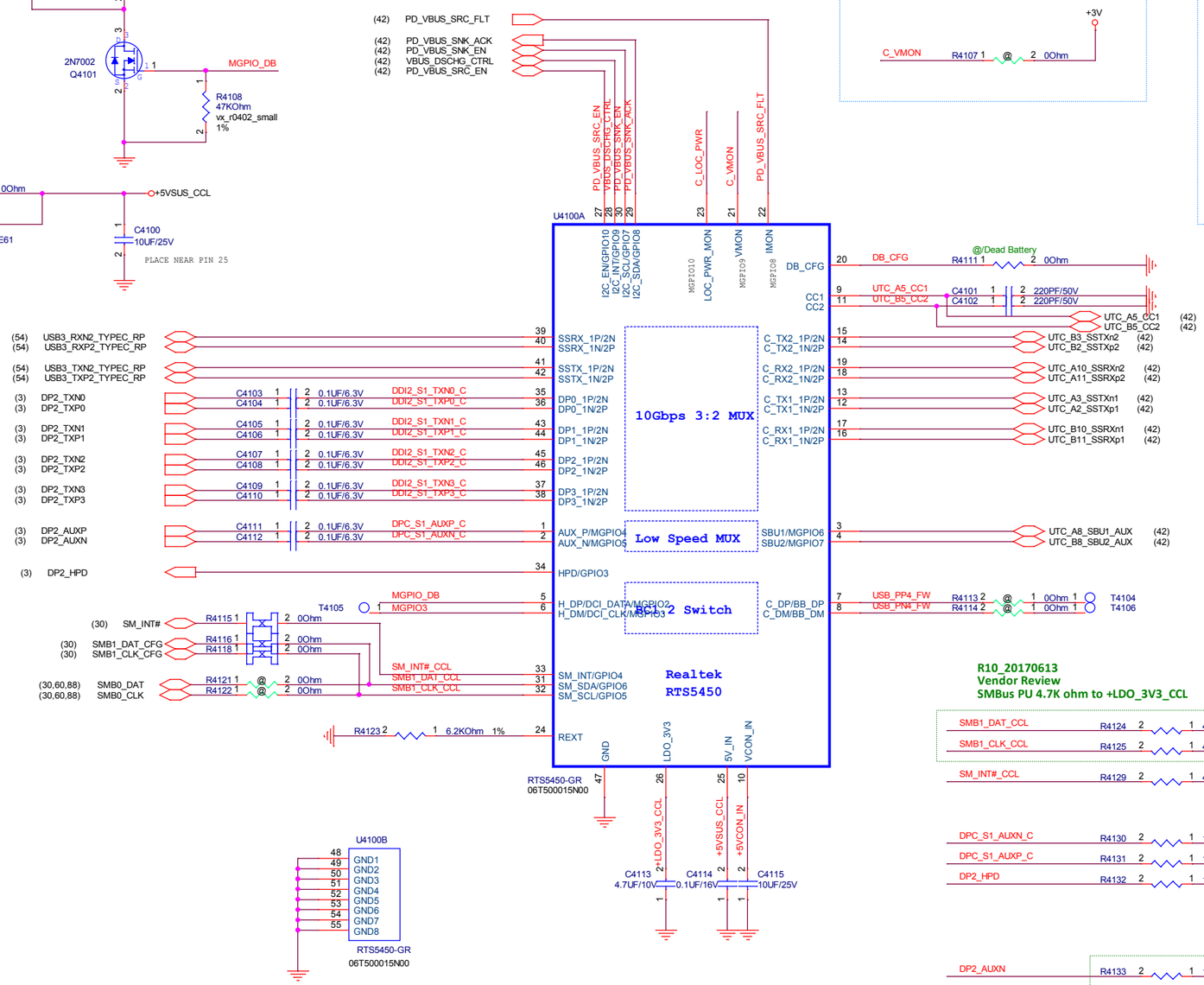
Size	Project Name	Rev
A	MILLER	1.4

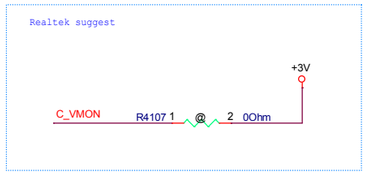
Date: Monday, June 11, 2018

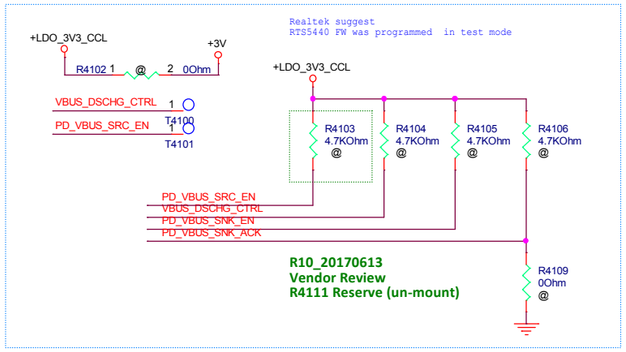
In case of 5V power source for VCON_IN is is equivalent grounded when OFF.
Q4101 is needed to isolate VCON_IN and 5V power source



	VBUS_DSCHG	SRC_PS_EN	SRC_PS_FLT	SNK_PS_EN	SNK_PS_ACK
5440	GPIO9/ MGPIO2	GPIO10	MGPIO8	GPIO7/ MGPIO3	GPIO8/ MGPIO1

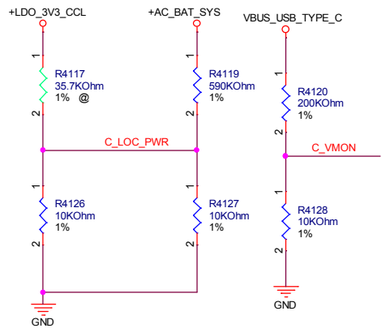




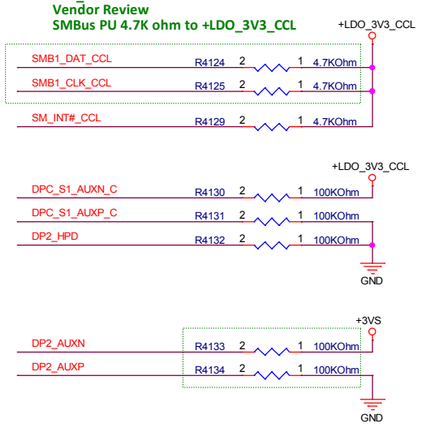


NOTE:
1.If the 5V_IN power supply voltage is fixed 5V or variable from 3.3V to 5V. Remove the 0ohm resistor.
2.If the 5V_IN power supply voltage is fixed 3.3V, stuff the 0ohm resistor

R10_20170613
Vendor Review
Mount R4115



R10_20170613
Vendor Review
SMBus PU 4.7K ohm to +LDO_3V3_CCL



Slave Addr	R4117	R4126
0XAC	NC	10K
0XAE	68.1K	10K
0XB0	35.7K	10K
0XB2	24.3K	10K

SMBus update FW 用addr_0

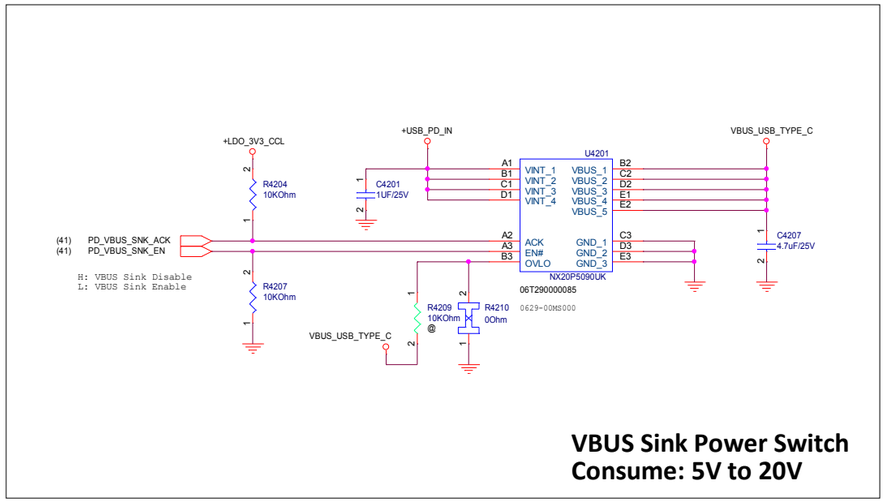
R4119, R4127, R4117, R4126 must be precision resistor of 1%.

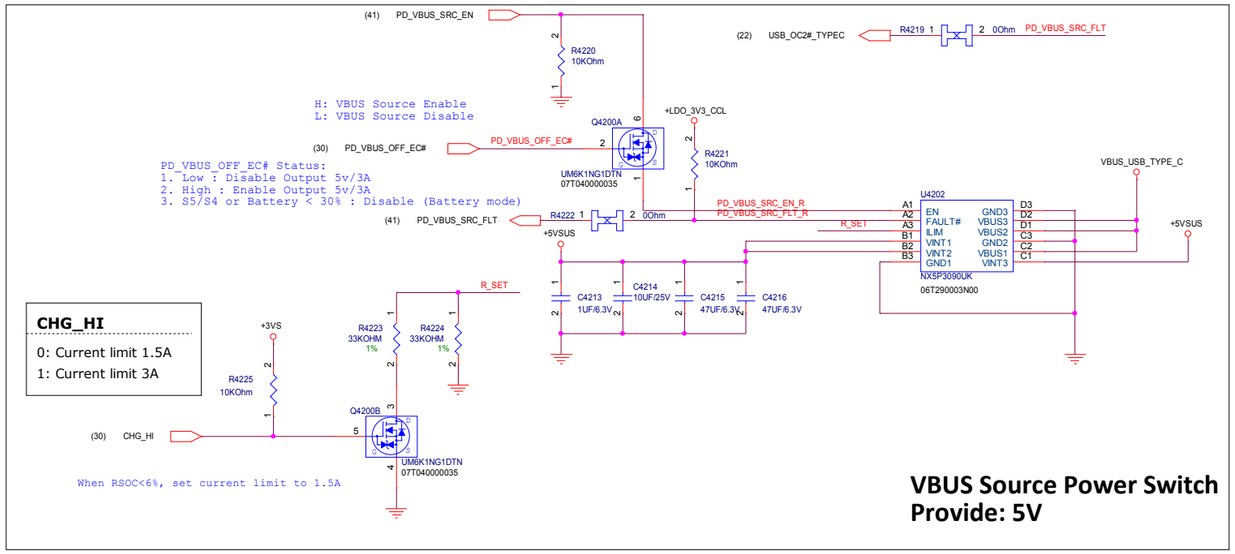
5450 meet PD 3.0 spec

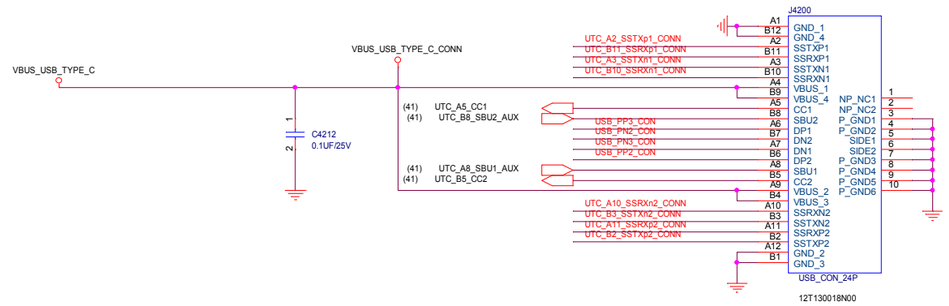
<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RTS5450
Engineer: Howard Chen
Size: C
Project Name: MILLER
Rev: 1.4
Date: Monday, June 11, 2018
Sheet 41 of 94

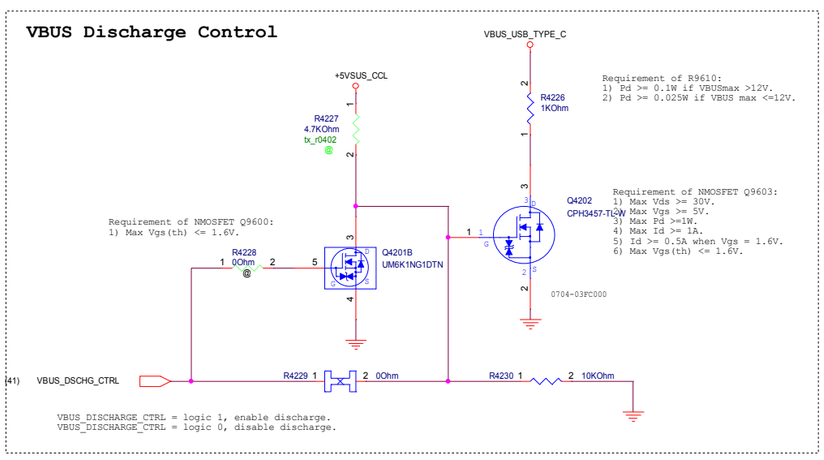


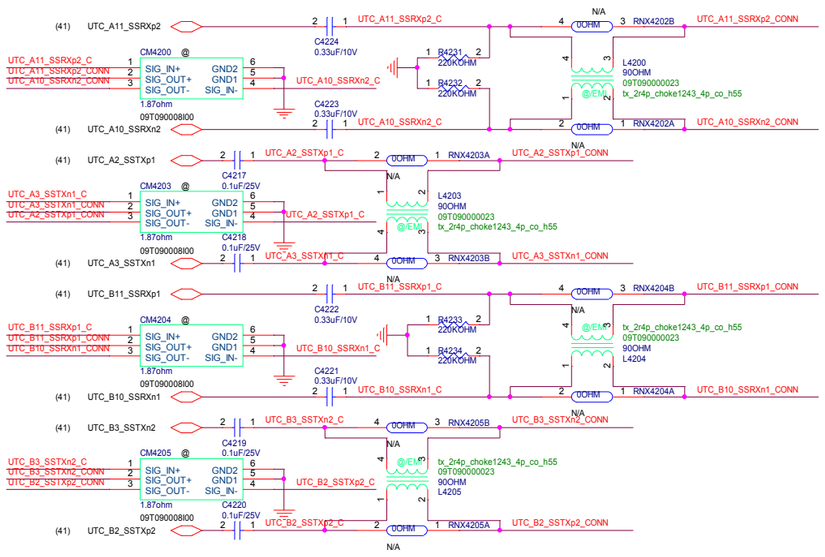




USB Type C Connector

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1





<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB-C Receptacle

Engineer: Howard Chen

Size	Project Name	Rev
Custom	MILLER	1.4

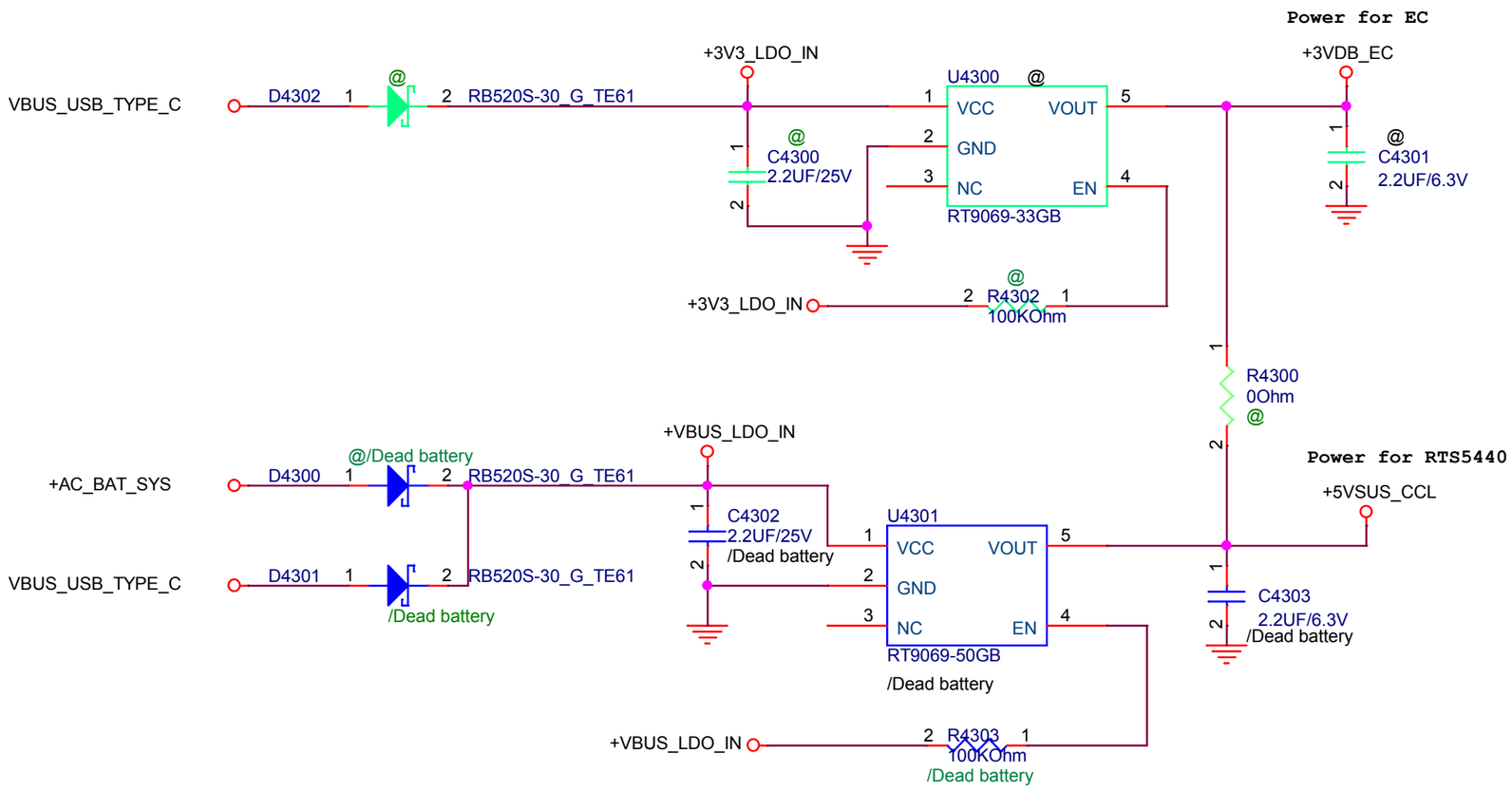
Date: Monday, June 11, 2018 Sheet 42 of 94

Hardware Solution For Dead Battery

For notebook applications, if the battery charger needs higher voltage than
5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C — VBUS_USB_TYPE_C (41,42)
+AC_BAT_SYS — +AC_BAT_SYS (41,45,80,81,82,83,85,87,88,91)
+3VDB_EC — +3VDB_EC (30)
+5VSUS_CCL — +5VSUS_CCL (41,42)

Requirement of U1:
1) Vin range: 4V-30V.
2) Vout: EC's operating voltage + Vf of D1
3) Output current >= EC's operating current.



<Variant Name>

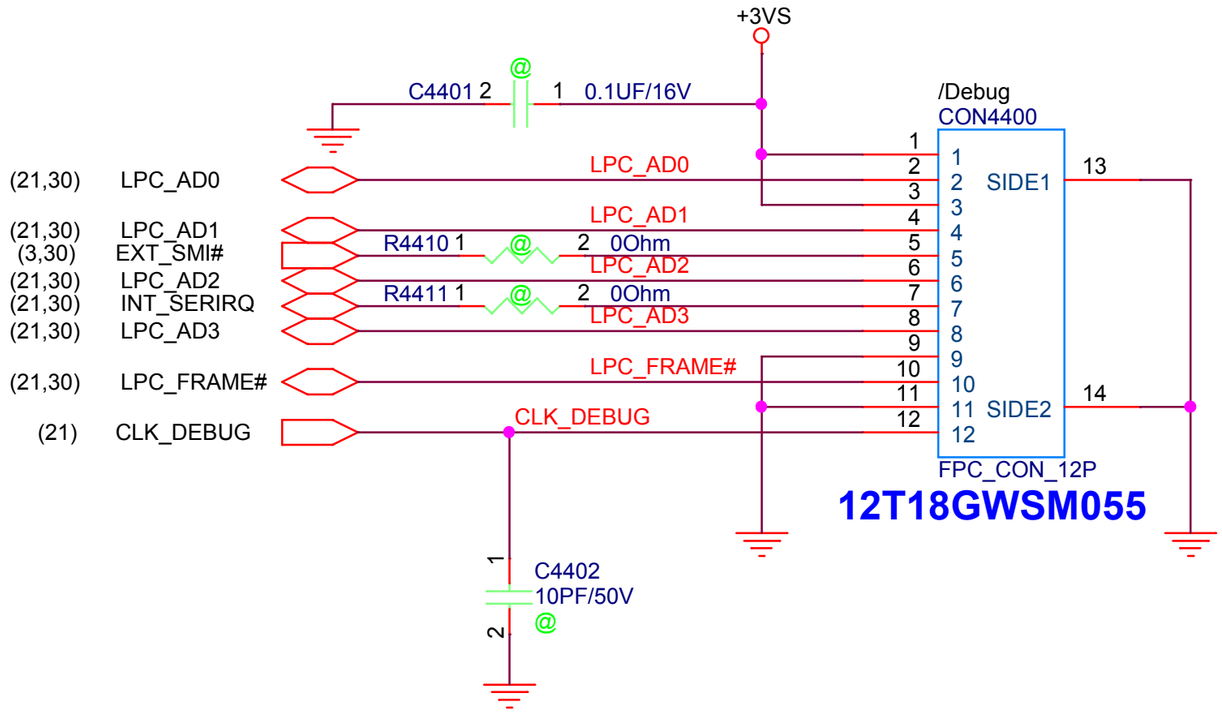
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Dead Battery

Engineer: Howard Chen

Size	Project Name	Rev
Custom	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 43 of 94



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DEBUG CONN.

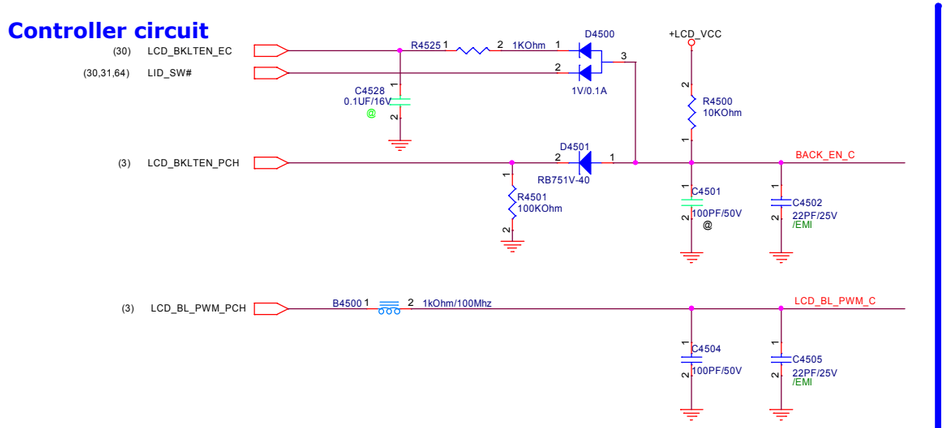
BG1/HW1

Engineer: Howard Chen

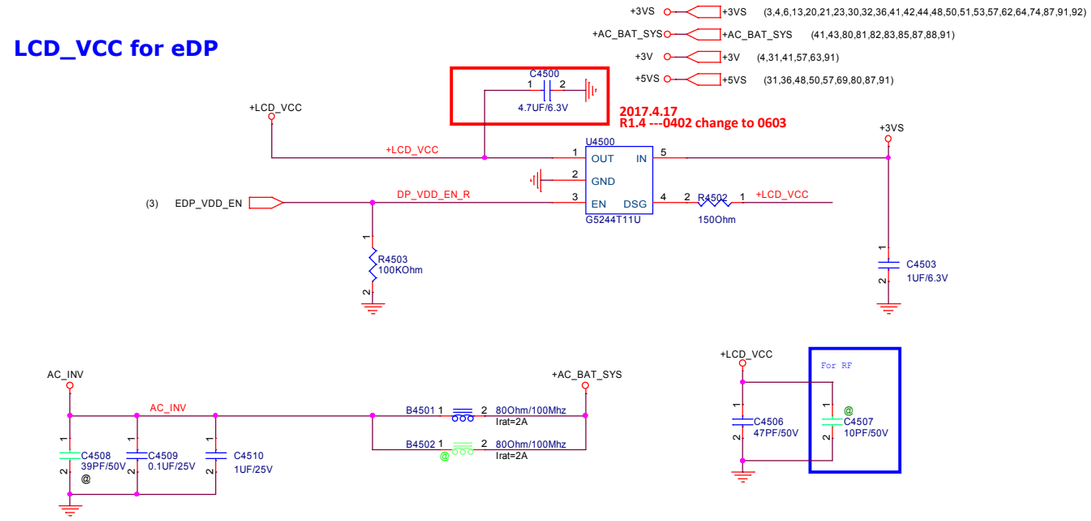
Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 44 of 94

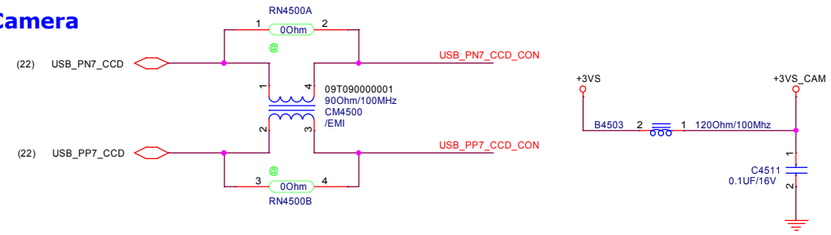
Controller circuit



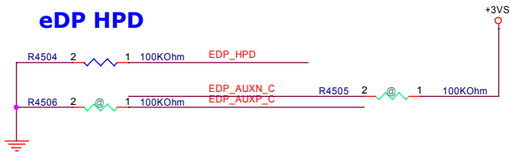
LCD_VCC for eDP



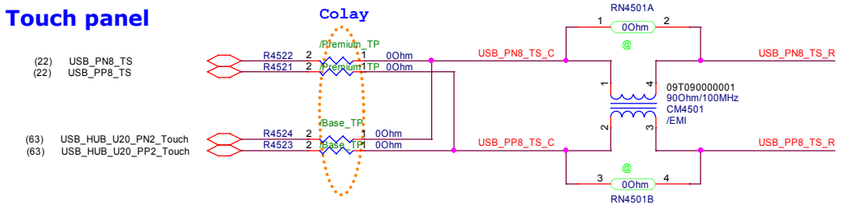
Camera

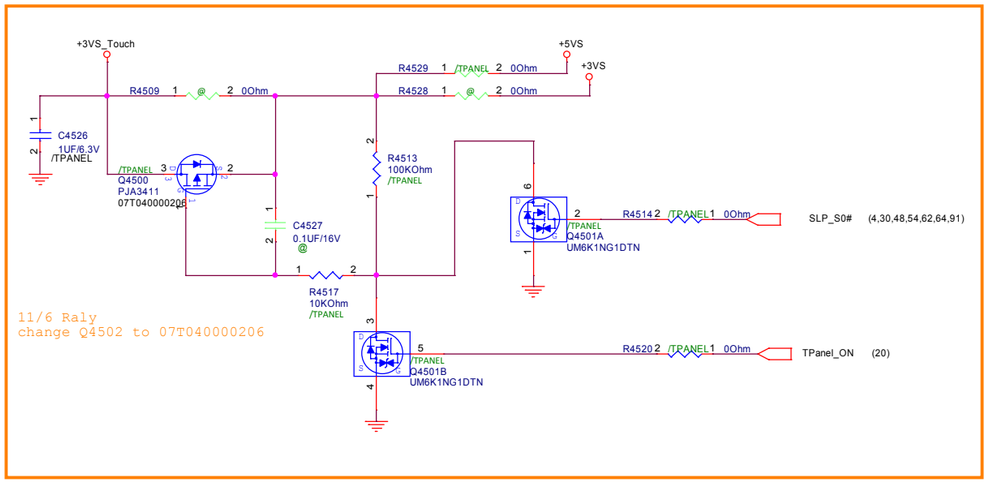


eDP HPD



Touch panel





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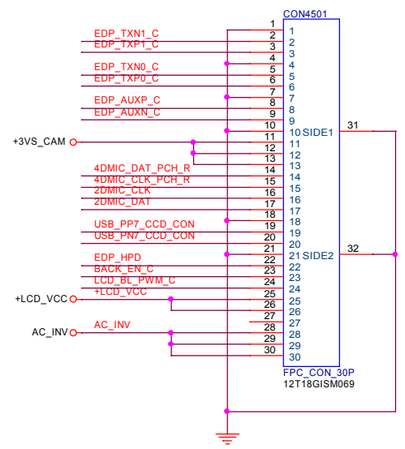
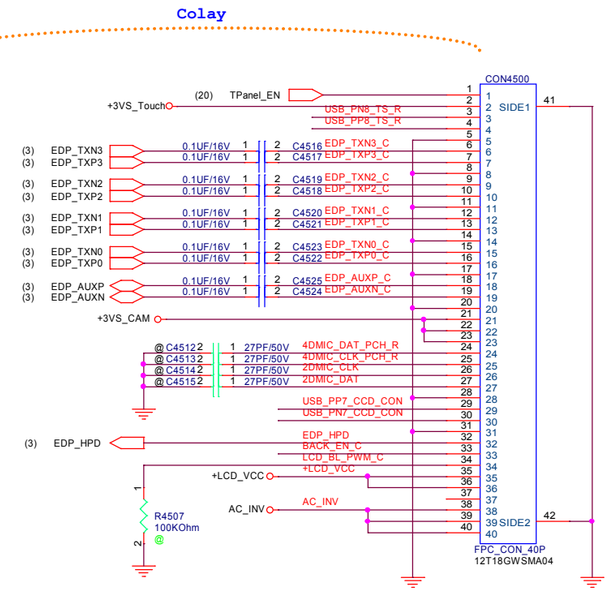
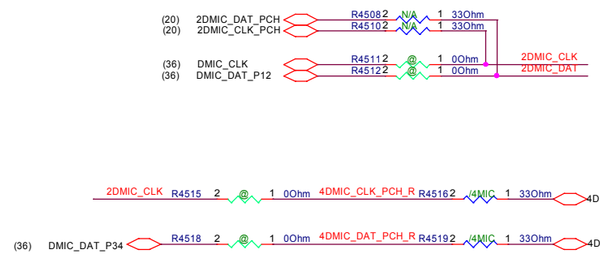






PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : eDP Out

BG1/HW1 Engineer: Howard Chen

Size	Project Name	Rev
Custom	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 45 of 94

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: *Howard Chen*

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

PEGATRON

Title : RSVD

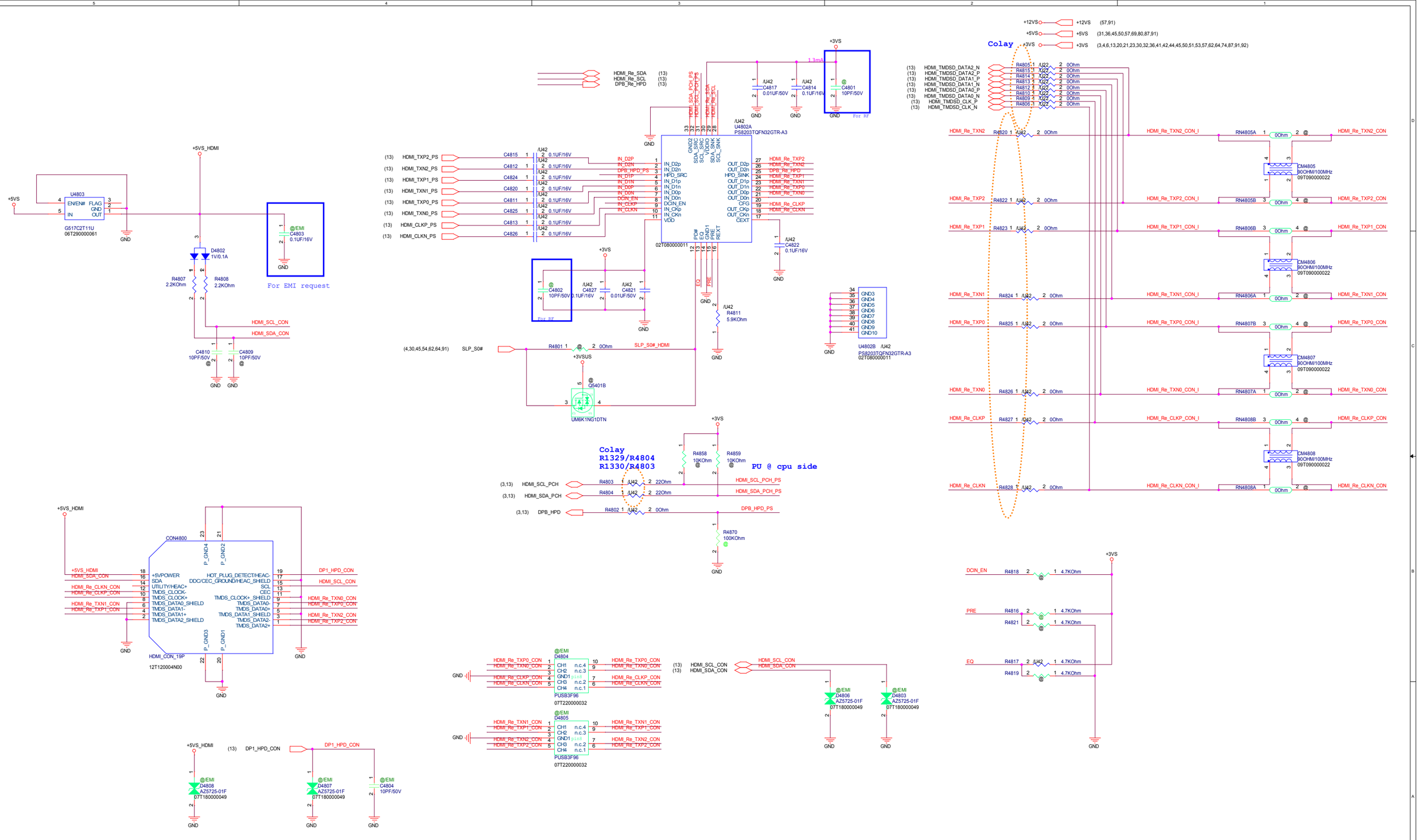
PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : HDMI-4K2K

BG1-HW3 RD

Engineer: Howard Chen

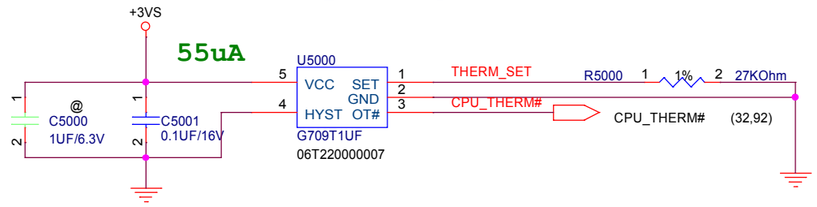
Size: Custom | Project Name: MILLER | Rev: 1.4

Date: Monday, June 11, 2018 | Sheet 48 of 94

5 4 3 2 1

D C B A

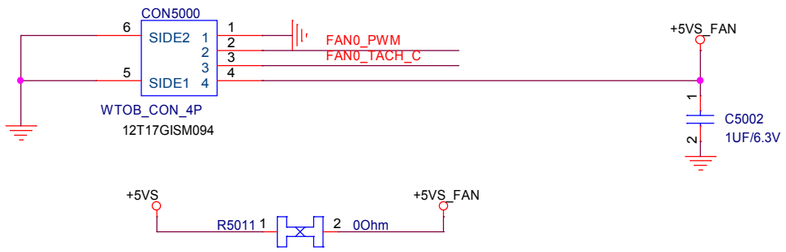
Thermal Sensor for package test

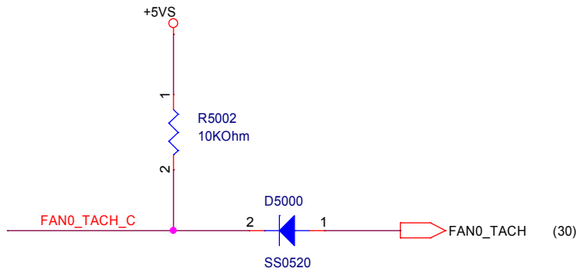


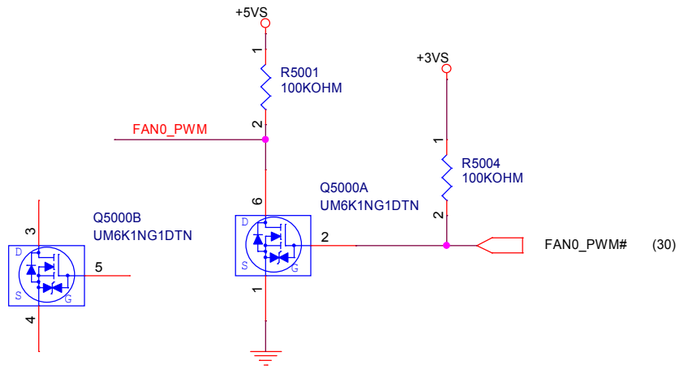
temp setting : 83 degree

RSET(kΩ)= 0.0012T2 - 0.9308T + 96.147

FAN

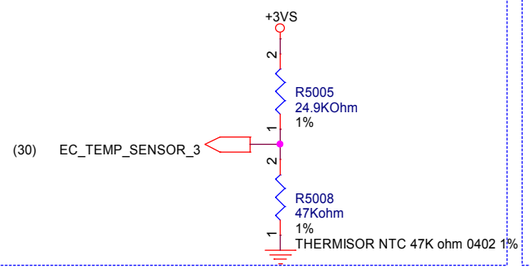




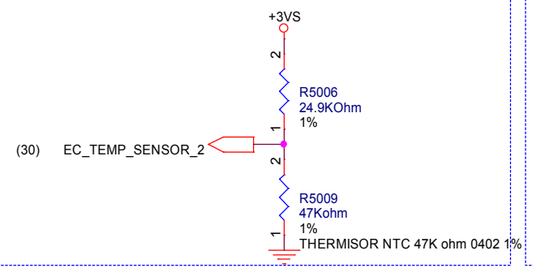


DPTF

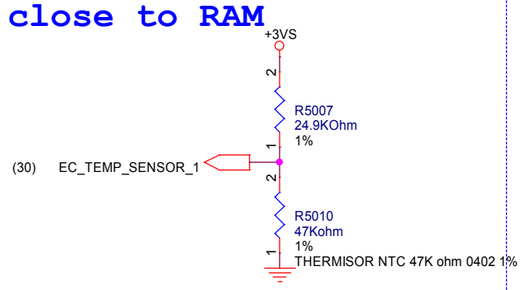
close to CPU VR



close to GPU VR

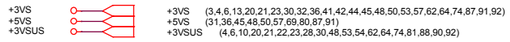


close to RAM



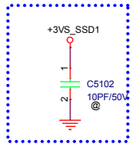
PEGATRON	Title : Thermal_Fan	
BG1/HW1	Engineer: Howard Chen	
Size: Custom	Project Name: MILLER	Rev: 1.4
Date: Monday, June 11, 2018	Sheet 50 of 94	

SATA SSD

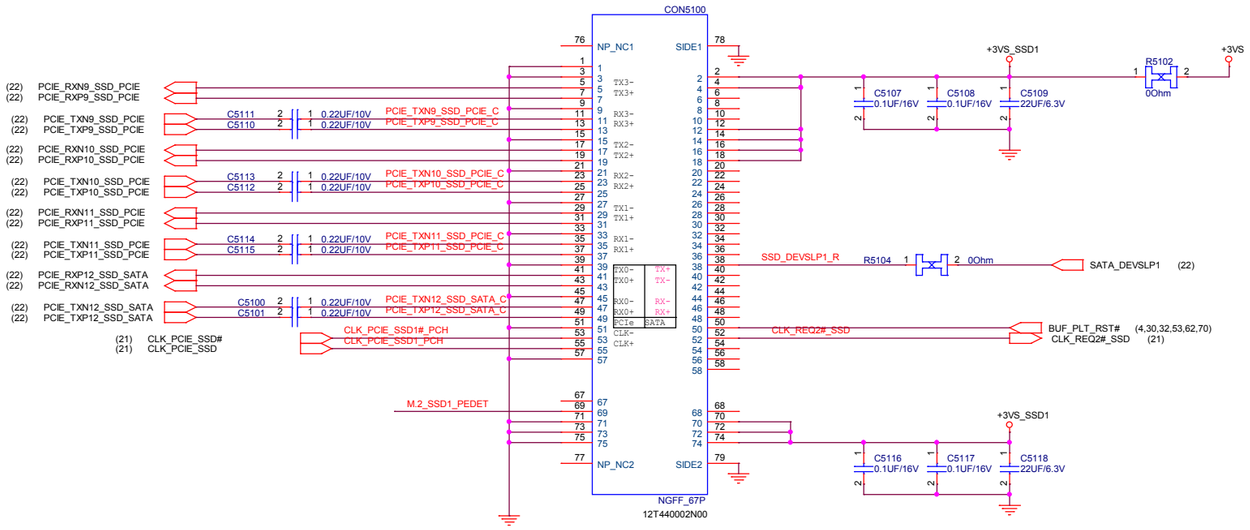


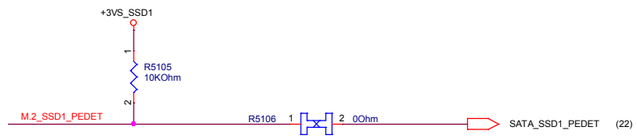
SATA / PCIe SSD

RF requirement



SSD





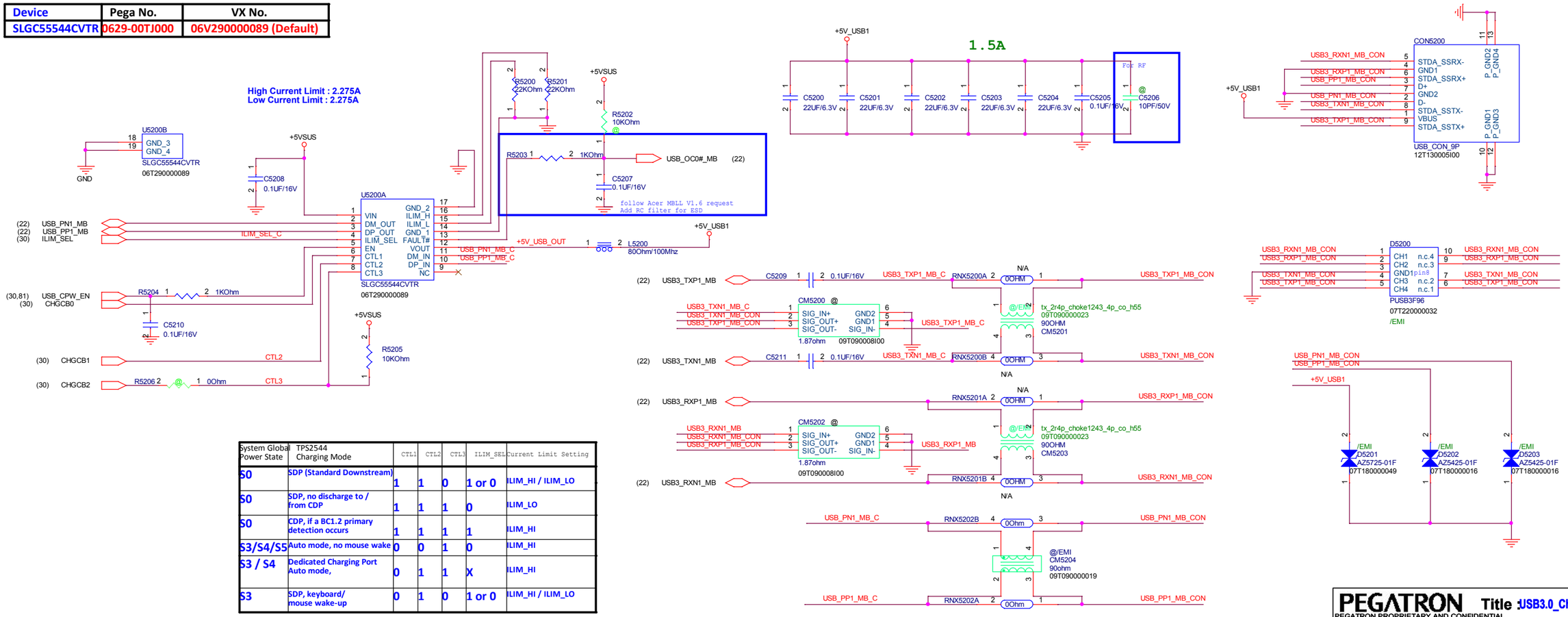
PEGATRON Title : SATA SSD_HDD
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD Engineer: Howard Chen

Size	Project Name	Rev
Custom	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 51 of 94

USB 3.0 ports x 1 with Sleep & Charge Left_Down

Device	Pega No.	VX No.
SLGC55544CVTR	0629-00TJ000	06V290000089 (Default)



System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3 / S4	Dedicated Charging Port Auto mode,	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW1

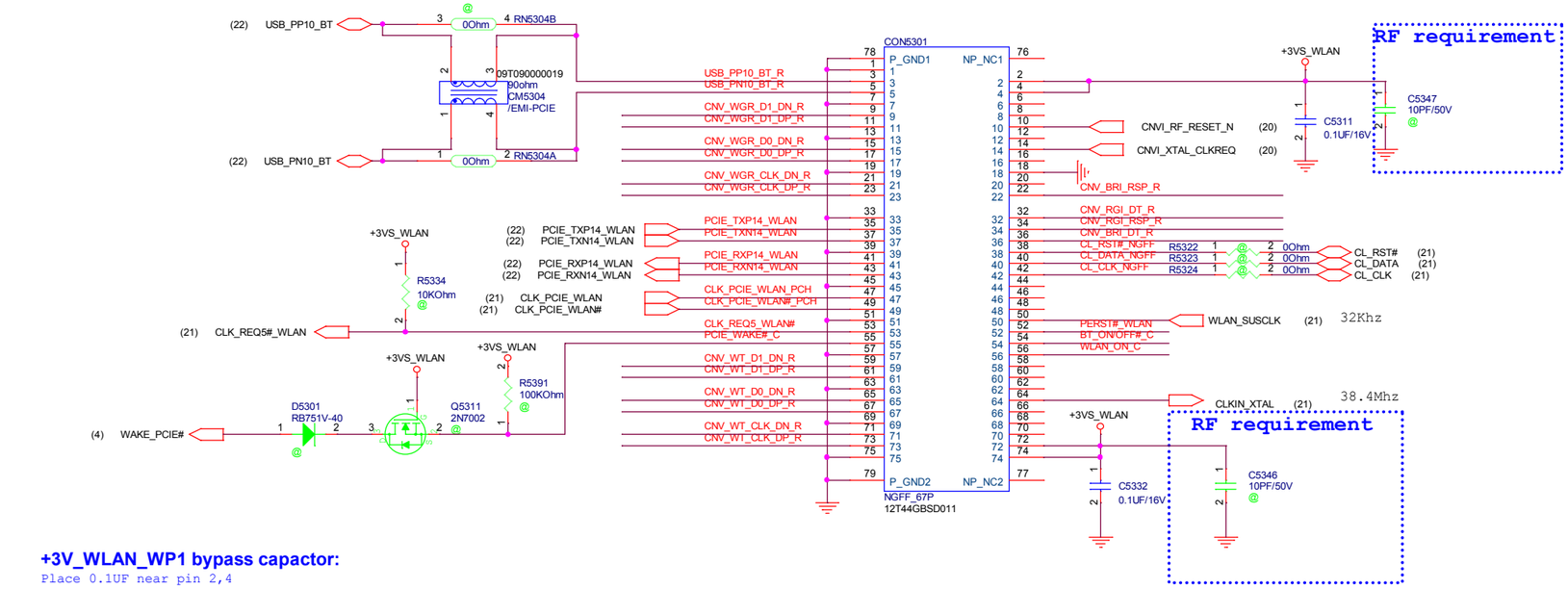
Title : USB3.0_Charge IC

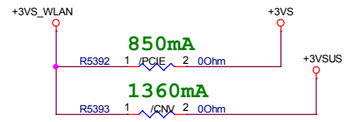
Engineer: Howard Chen

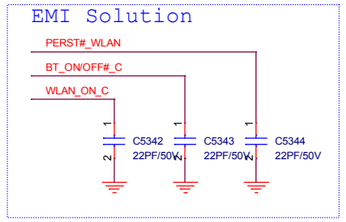
Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 52 of 94

M.2 Key.E WIFI CONNECTOR



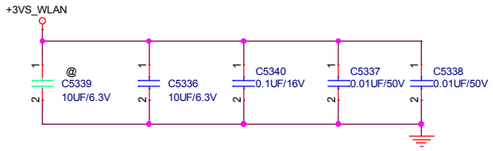


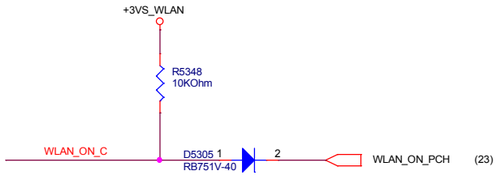


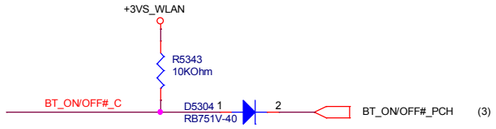
+3V_WLAN_WP1 bypass capactor:

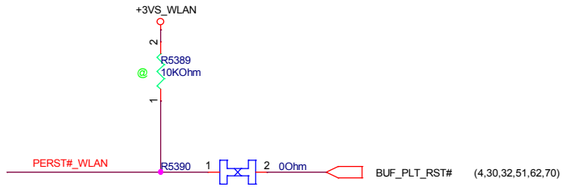
Place 0.1UF near pin 2,4

Place 10UF near +3V_WLAN_WP1 source side.



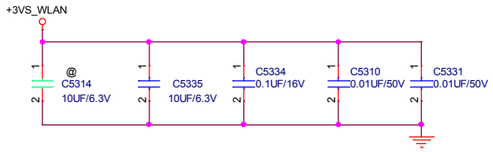




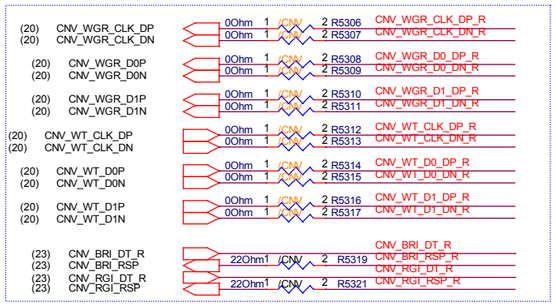


Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.



CNVi



PEGATRON Title : PCIE_WLAN_BT

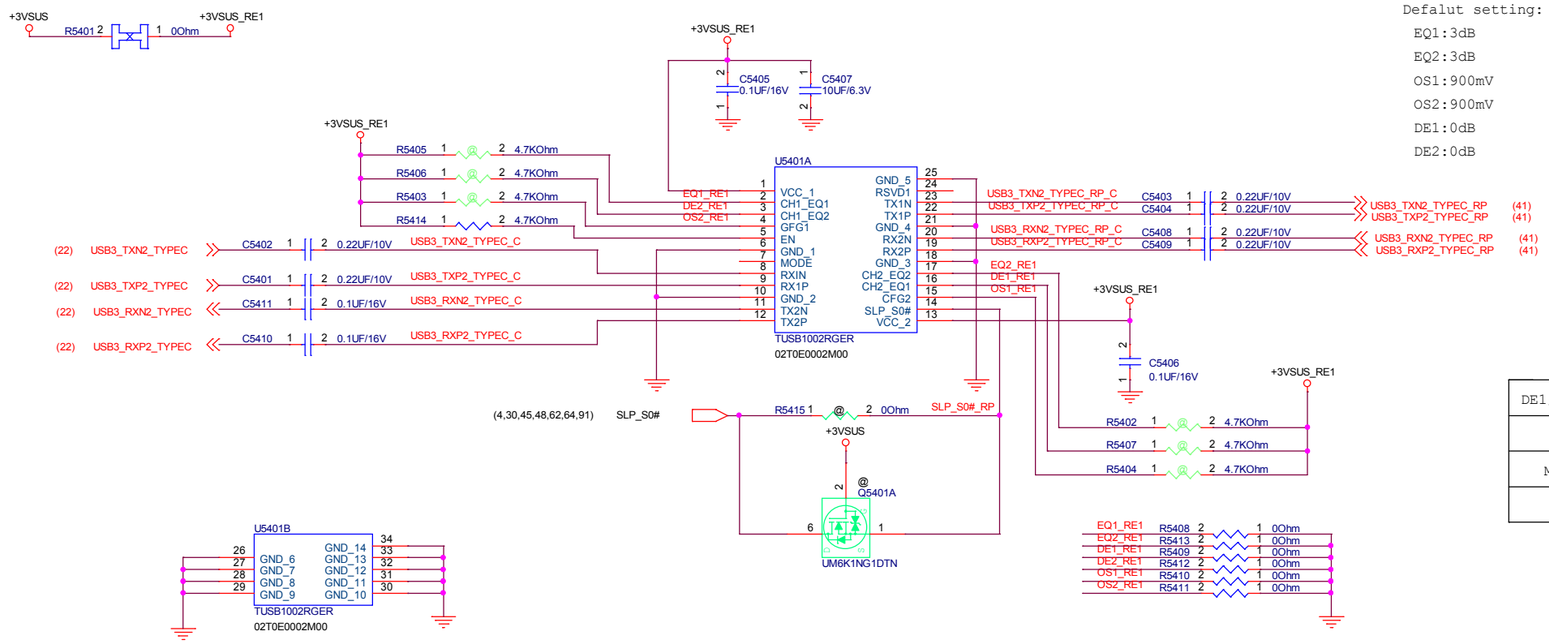
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1 Engineer: Howard Chen

Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 53 of 94

USB3.0 re-driver (gen2)



Defalut setting:

EQ1:3dB
EQ2:3dB
OS1:900mV
OS2:900mV
DE1:0dB
DE2:0dB

Equalizer control

EQ1/EQ2	Channel 1/Channel 2
L	3 dB
Mid	6 dB
H	9 dB

OS1/OS2	Channel 1/Channel 2
L	900mV
H	1100mV

De-emphasis control

DE1/DE2	OS1=0 /OS2=0	DE1/DE2	OS1=1 /OS2=1
L	0 dB	L	-2.6 dB
Mid	-3.5 dB	Mid	-5.9 dB
H	-6.2 dB	H	-8.3 dB

PEGATRON Title : USB3 GEN2 redriver

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: Howard Chen

Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 54 of 94

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

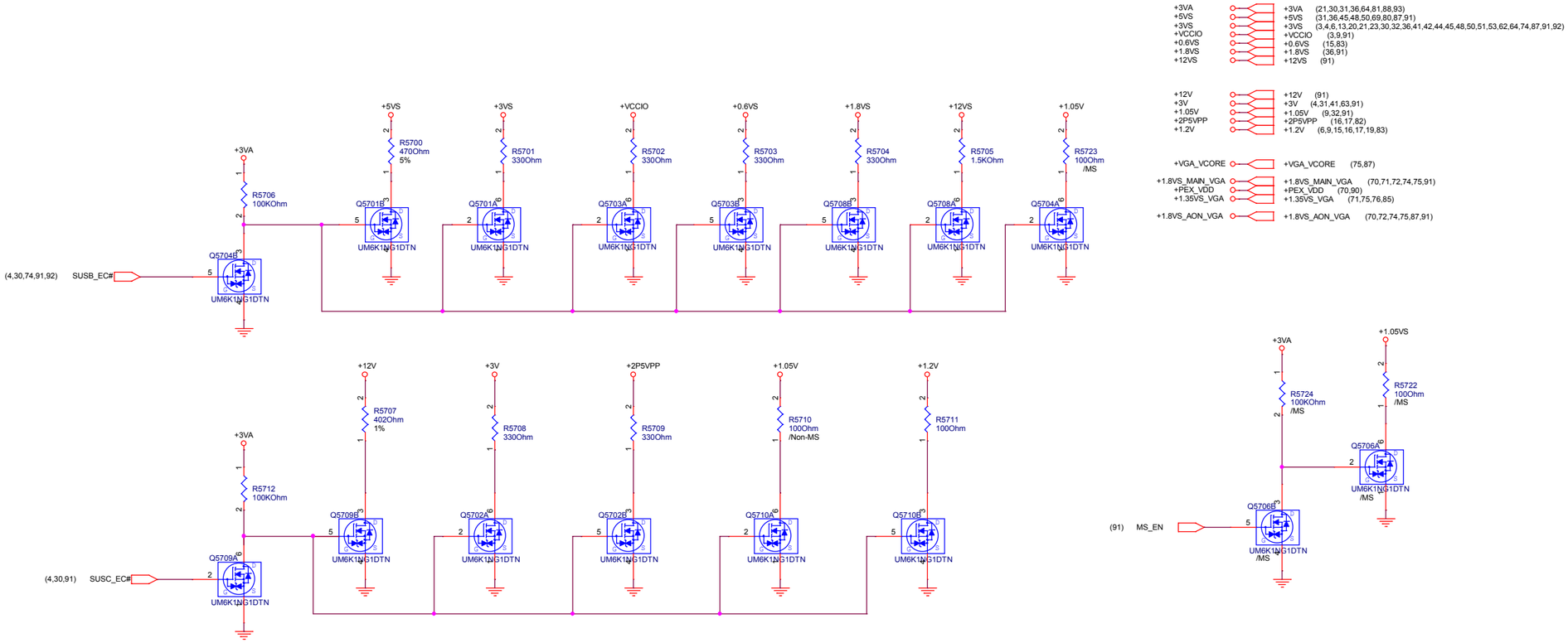
Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

5 4 3 2 1

D C B A



PEGATRON Title : DISCHARGE

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW1 Engineer: Howard Chen

Size	Project Name	Rev
Custom	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 57 of 94

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

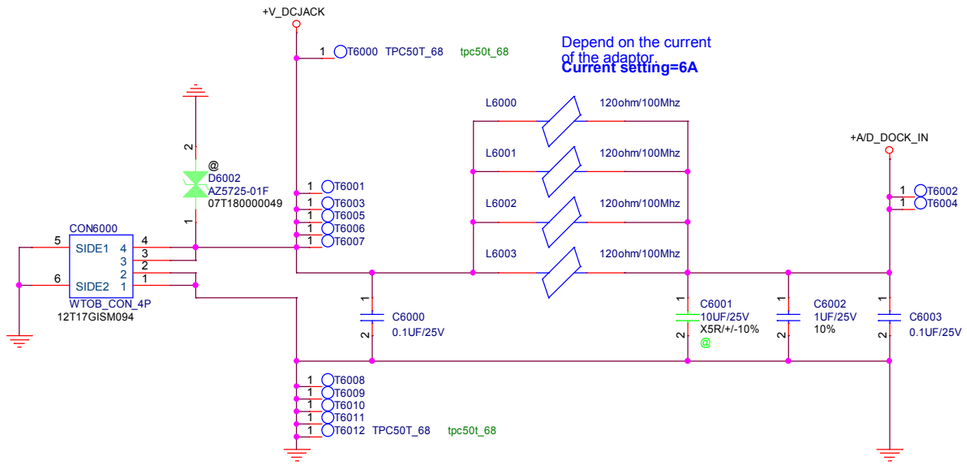
<OrgName>

Engineer: Howard Chen

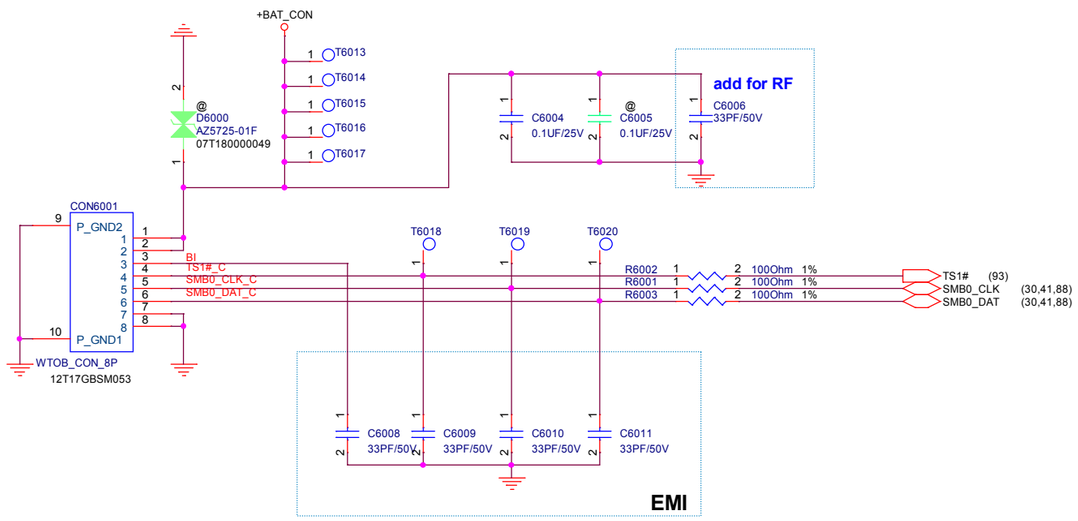
Size	Project Name	Rev
A	MILLER	1.4

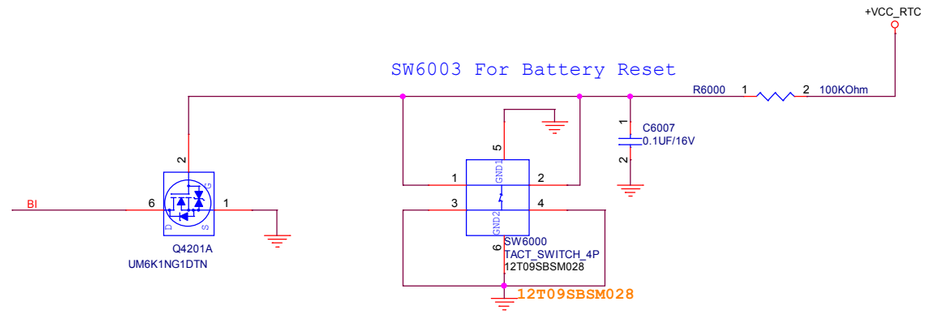
Date: Monday, June 11, 2018

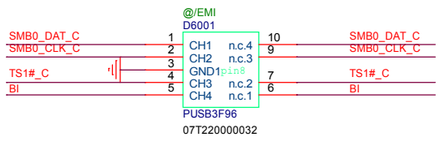
DC Jack WTB CONN



Battery Connector







PEGATRON	Title : DC_BAT_CONN	
BG1/HW1	Engineer: Howard Chen	
Size: Custom	Project Name: MILLER	Rev: 1.4
Date: Monday, June 11, 2018	Sheet 60 of 94	

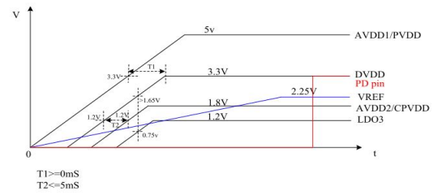
Touch Panel & Camera

AUDIO CODEC

SSD1&SSD2

AUDIO CODEC

WLAN



CardReader & USB Hub

FingerPrint & Touch Pad

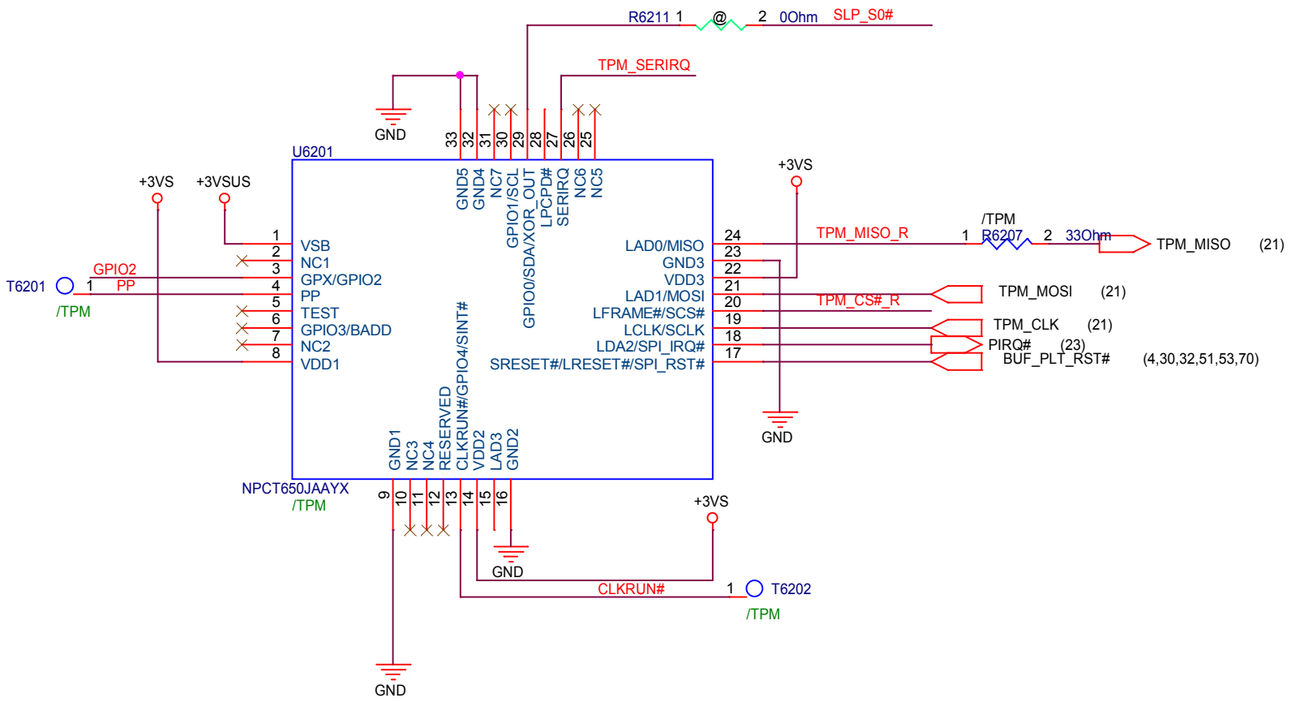
PEGATRON Title : PWR_SW

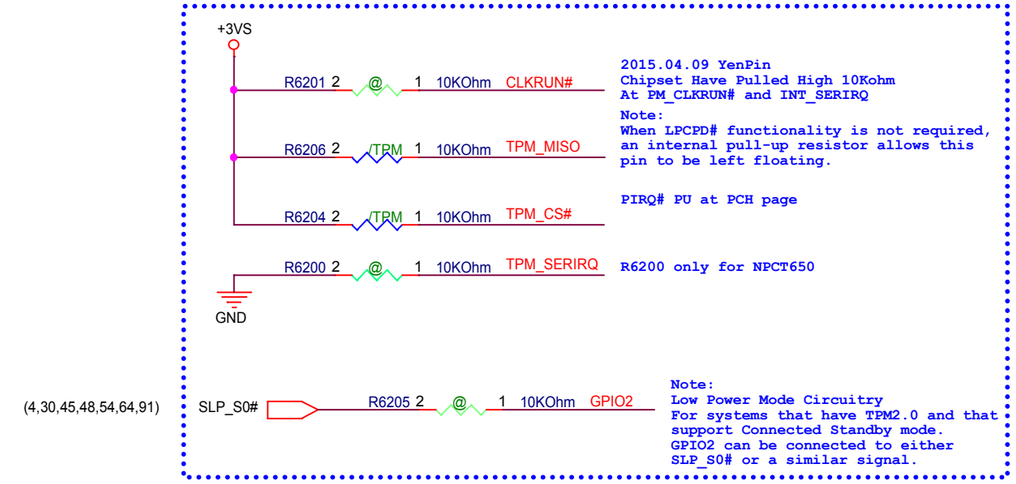
BG1/HW1 Engineer: Howard Chen

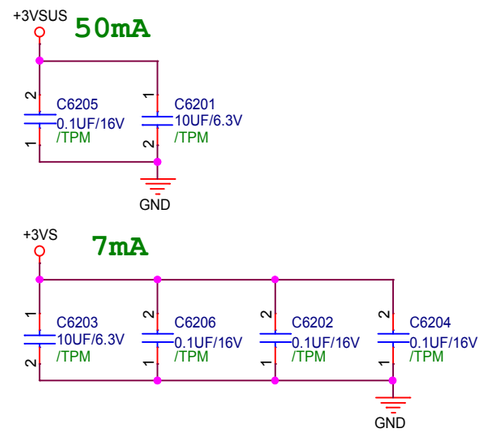
Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 61 of 94

62 TPM NPCT650/750 - SPI

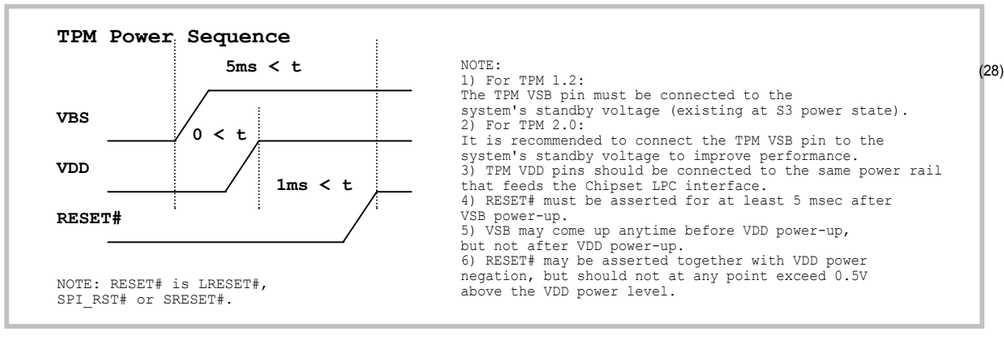


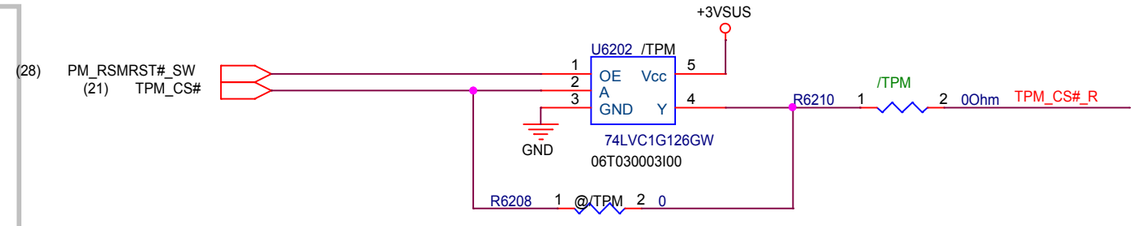




TPM

VDD: Power the I/O buffers of the GPIO ports and the Host Interface
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.

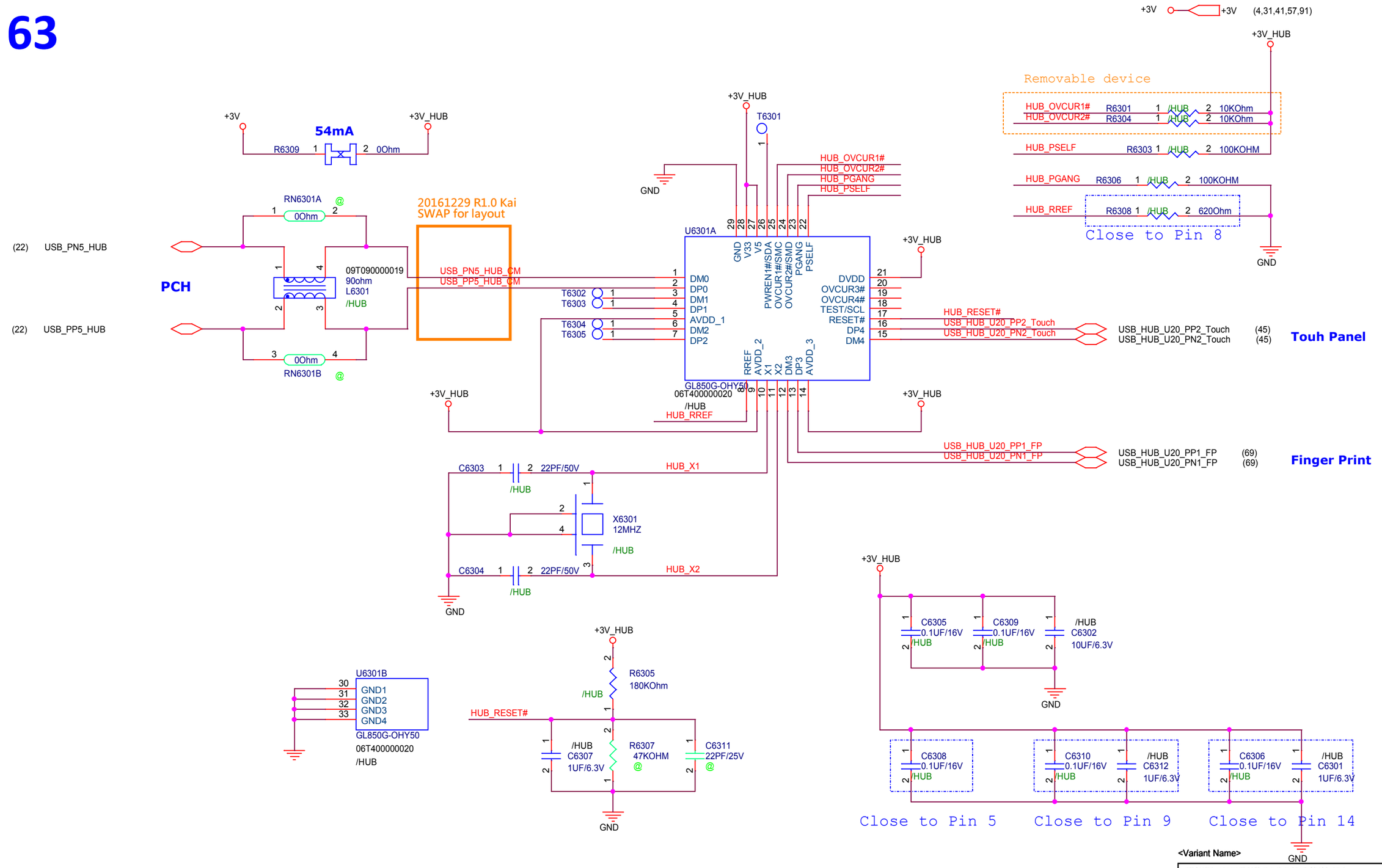




PEGATRON Title : TPM NPCT650
BG1-HW3 RD Engineer: Howard Chen

Size	Project Name	Rev
B	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 62 of 94



<Variant Name>

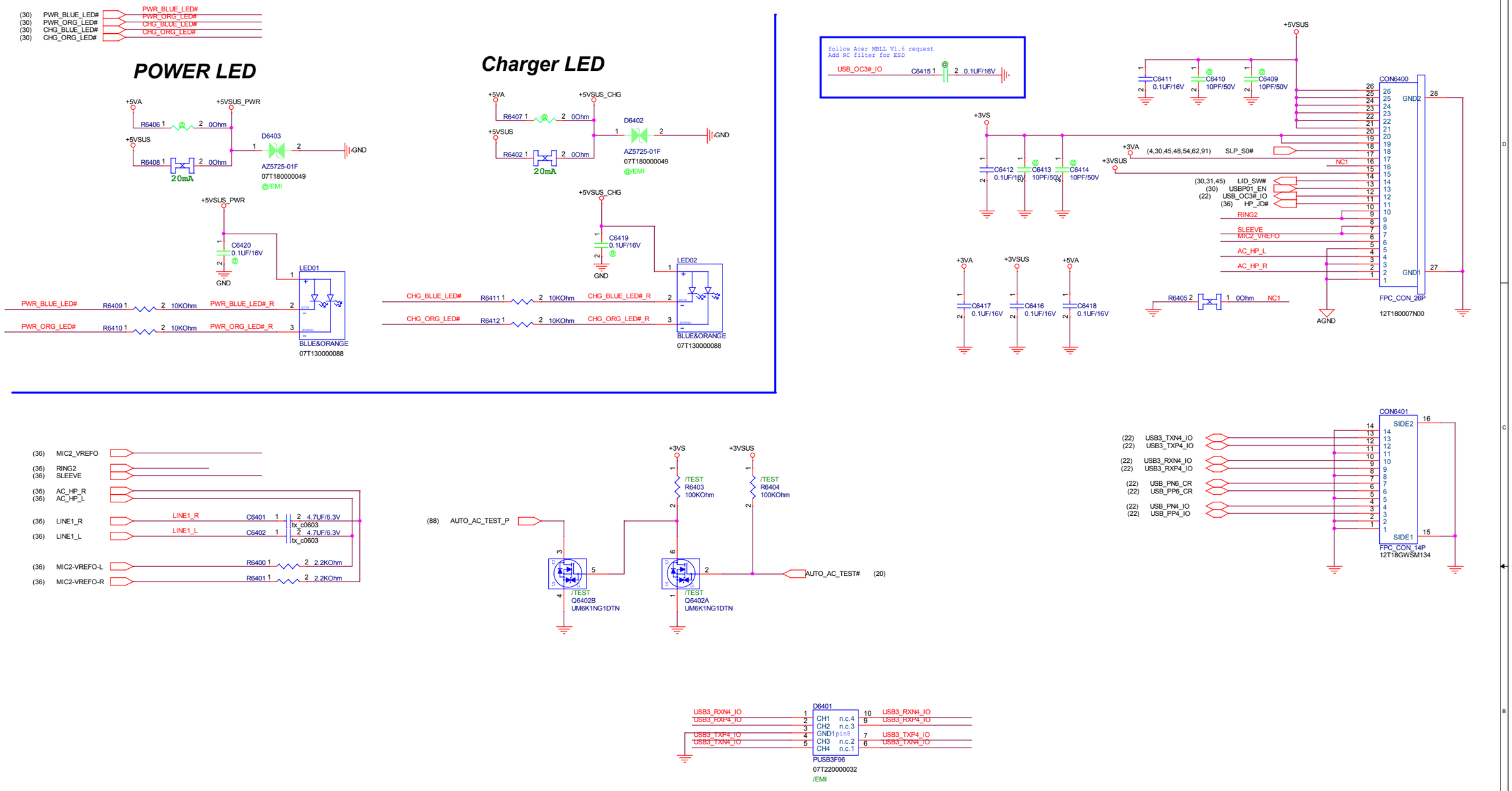
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB 2.0 Hub

Engineer: Howard Chen

Size	Project Name	Rev
B	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 63 of 94



PEGATRON Title : IO Bd Connector

BG1-HW3 RD Engineer: Howard Chen

Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 64 of 94

<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RSVD

Engineer: *Howard Chen*

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

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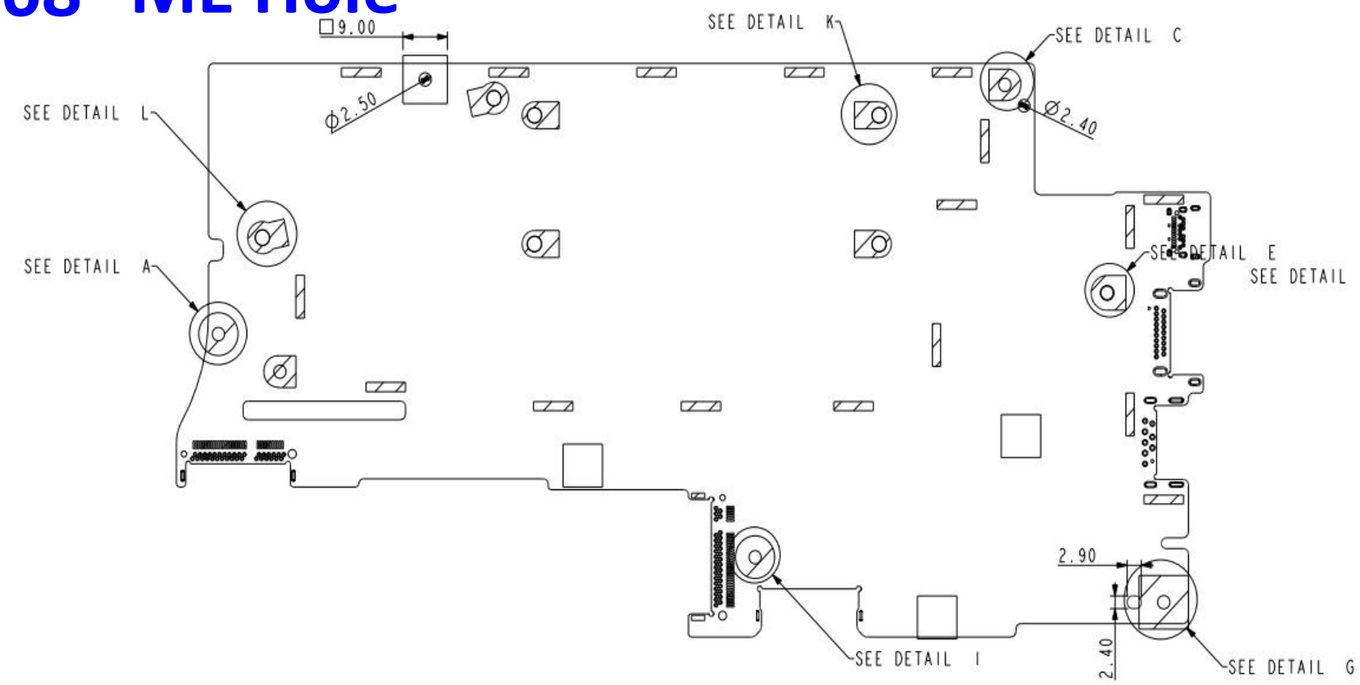
5 4 3 2 1

D C B A

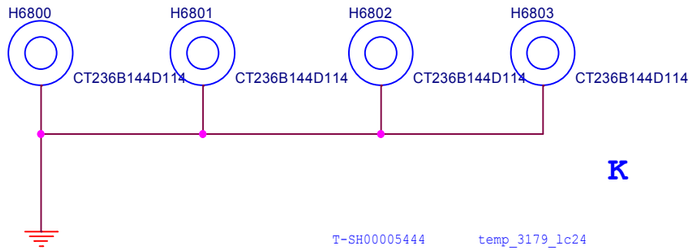
5 4 3 2 1

D C B A

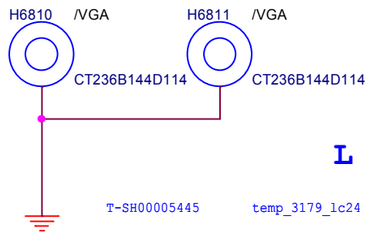
68 ME Hole



CPU NUT

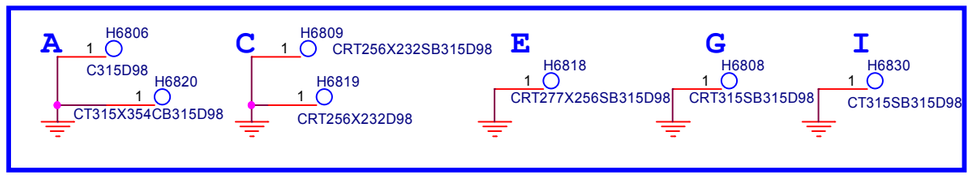


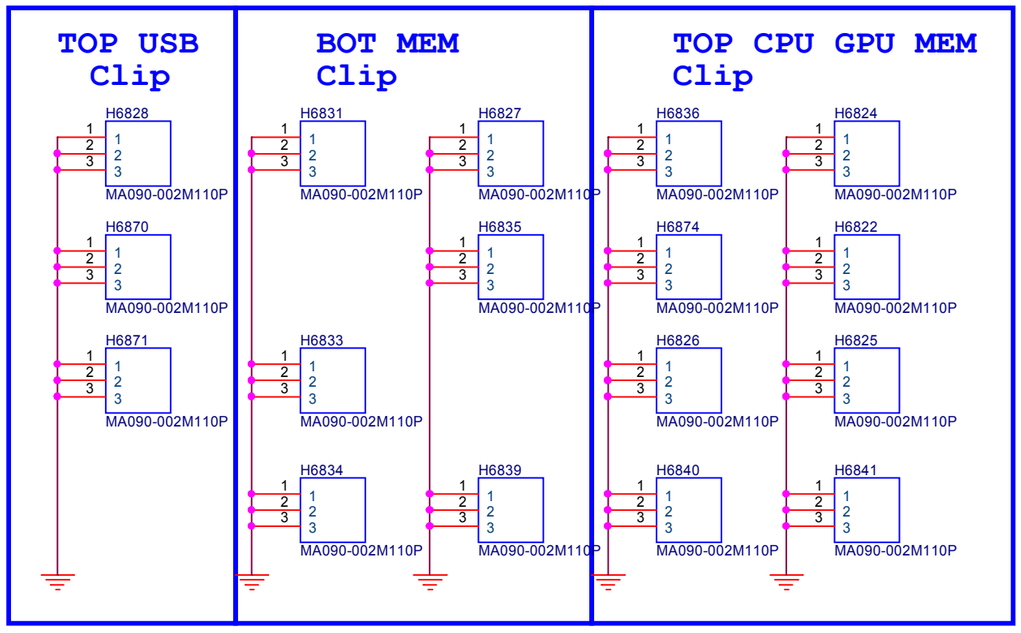
GPU NUT



npth 定位孔

s00111





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

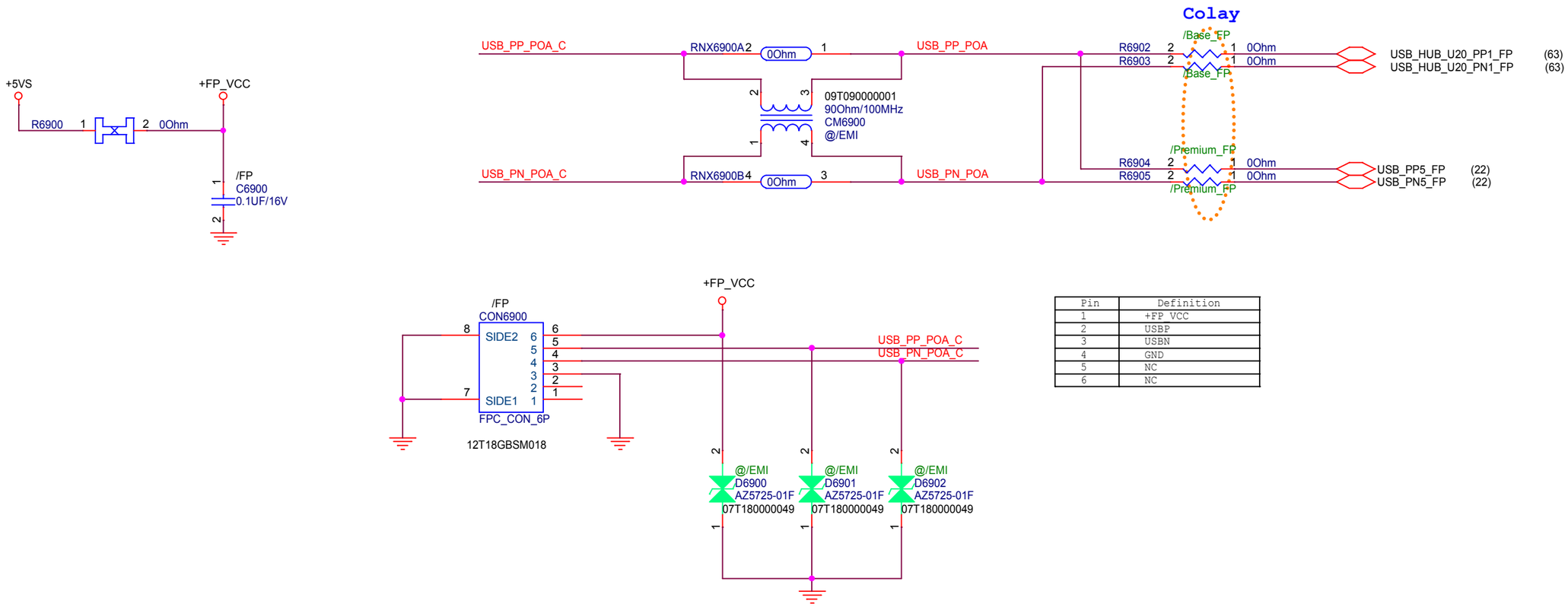
Title : ME Hole

BG1/HW1

Engineer: Howard Chen

Size	Project Name	Rev
Custom	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 68 of 94



Pin	Definition
1	+FP_VCC
2	USBP
3	USBN
4	GND
5	NC
6	NC

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Finger printer

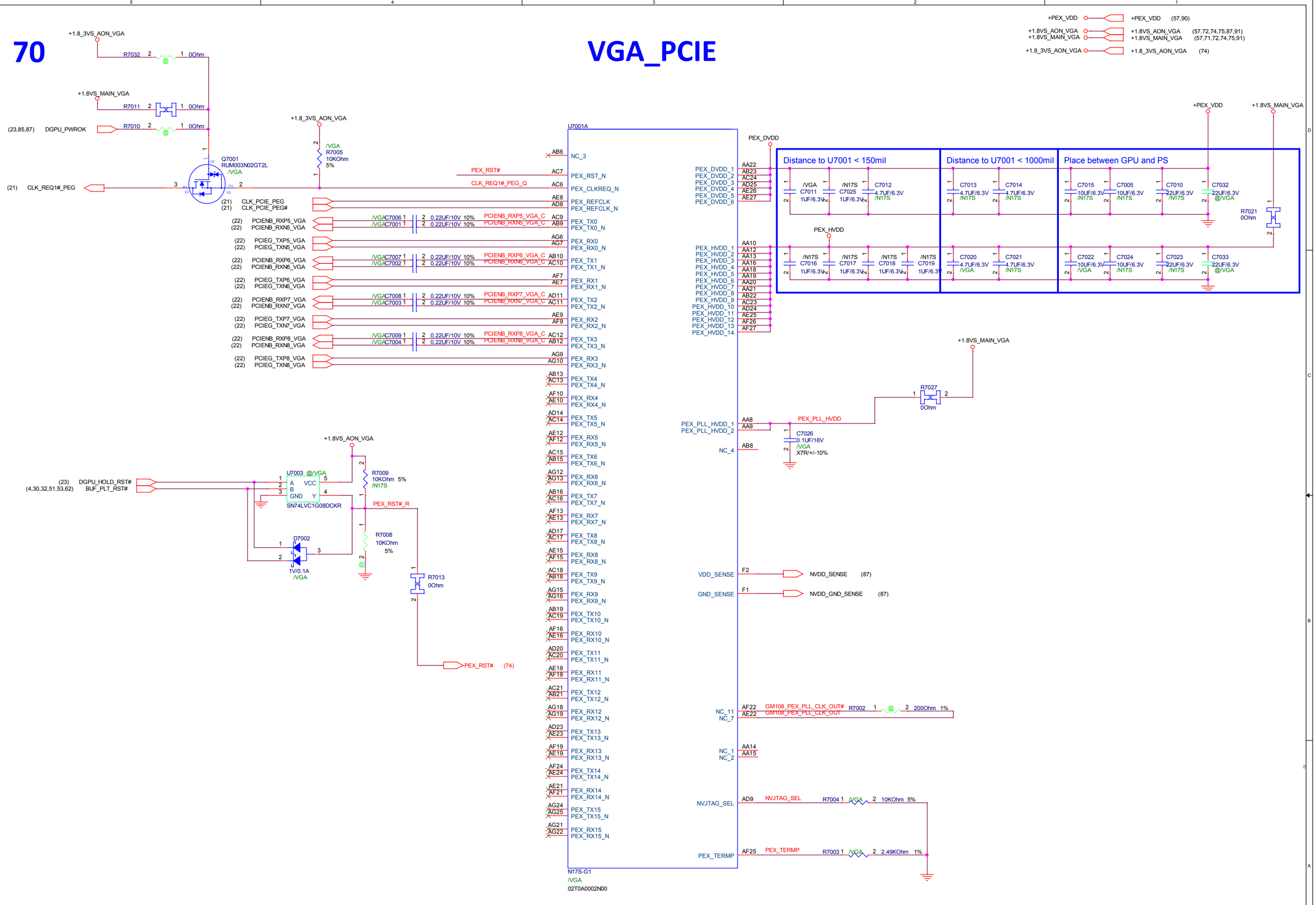
BG1/HW1

Engineer: Howard Chen

Size	Project Name	Rev
B	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 69 of 94

VGA_PCIE



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : VGA_PCIE

Engineer: Howard Chen

BG1/HW1

Size	Project Name	Rev
C	MILLER	1.4

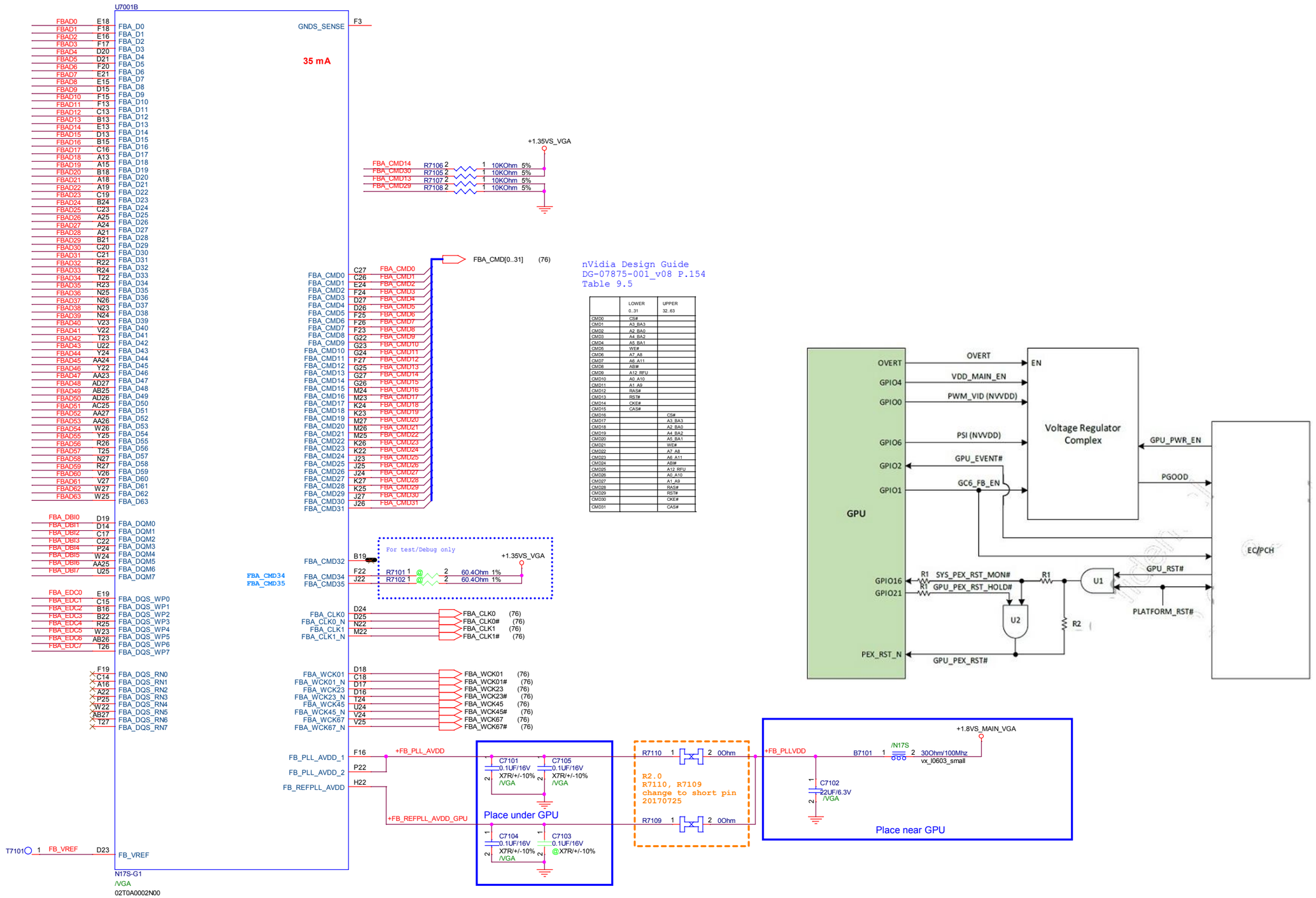
Date: Monday, June 11, 2018 Sheet 70 of 94

VGA_FRAME BUFFER_GDDR5

(76) FBAD[0..63]
(76) FBA_DBI[0..7]
(76) FBA_EDC[0..7]

+1.35VS_VGA
+1.8VS_MAIN_VGA
+PEX_VDD

+1.35VS_VGA (57,75,76,85)
+1.8VS_MAIN_VGA (57,70,72,74,75,91)
+PEX_VDD (57,70,90)



nVidia Design Guide
DG-07875-001_v08 P.154
Table 9.5

	LOWER 0..31	UPPER 32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : VGA_FRAME BUFFER

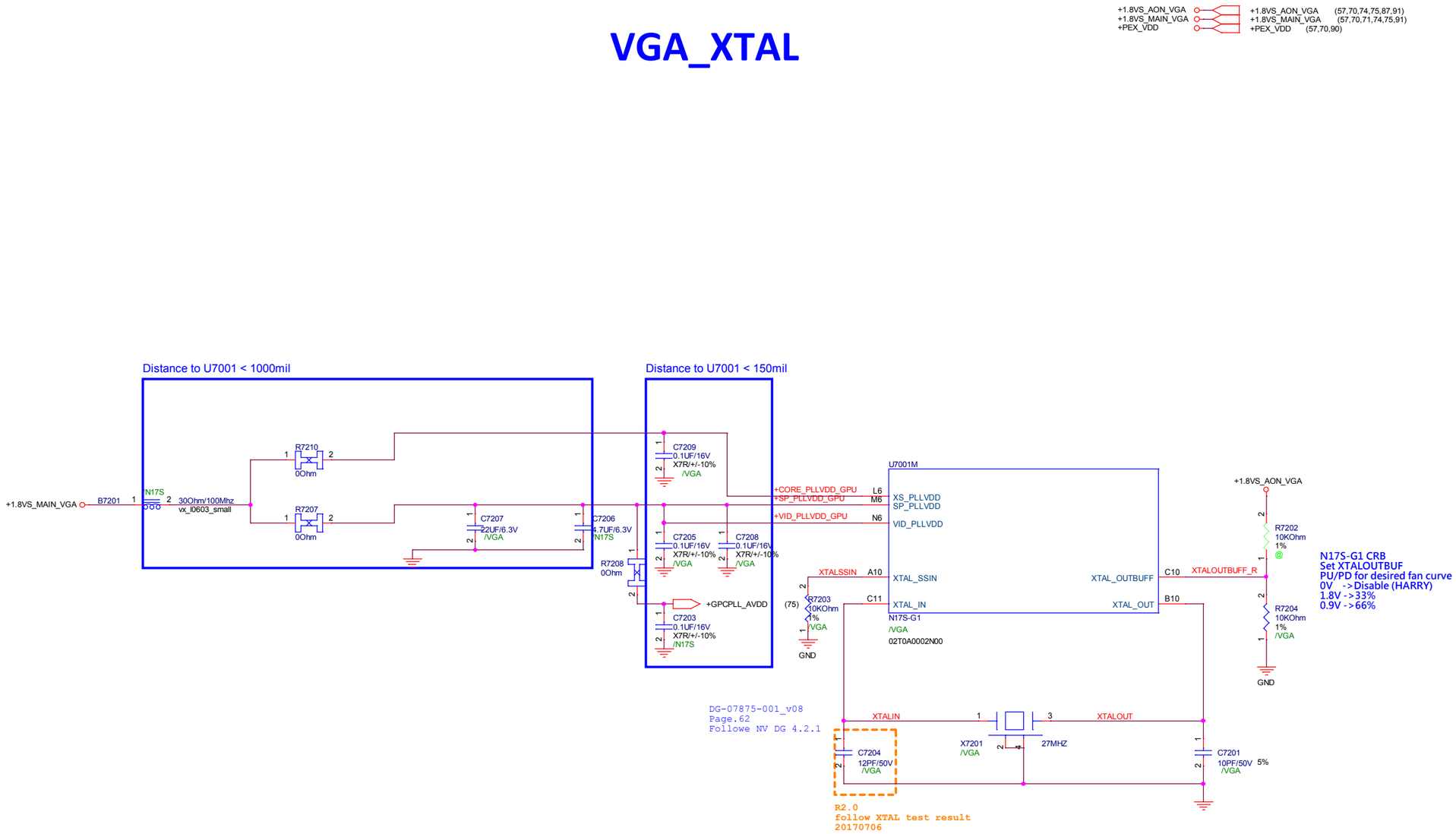
Engineer: Howard Chen

BG1/HW1

Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 71 of 94

VGA_XTAL



PEGATRON Title : VGA_XTAL

PEGATRON PROPRIETARY AND CONFIDENTIAL

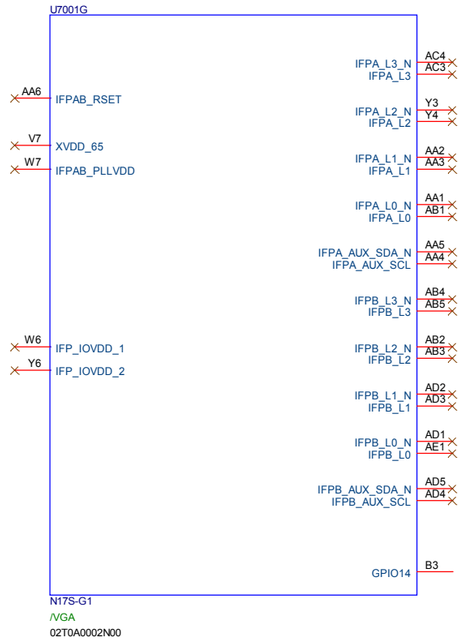
Engineer: Howard Chen

BG1/HW1

Size	Project Name	Rev
C	MILLER	1.4

Date: Monday, June 11, 2018 Sheet 72 of 94

VGA_DISPLAY



DG 10.2.1 Table 10.2
GB2C-64 no display support

Table 10.2 GB2C-64 Standard Configurations

Link	Standard Display Configurations
Note: GPUs in GB2C-64 packages provide no display links and no display head support; they are operated in Optimus/MS-Hybrid mode. **Note**: GPUs in GB2C-64 packages do not support G-SYNC™.	

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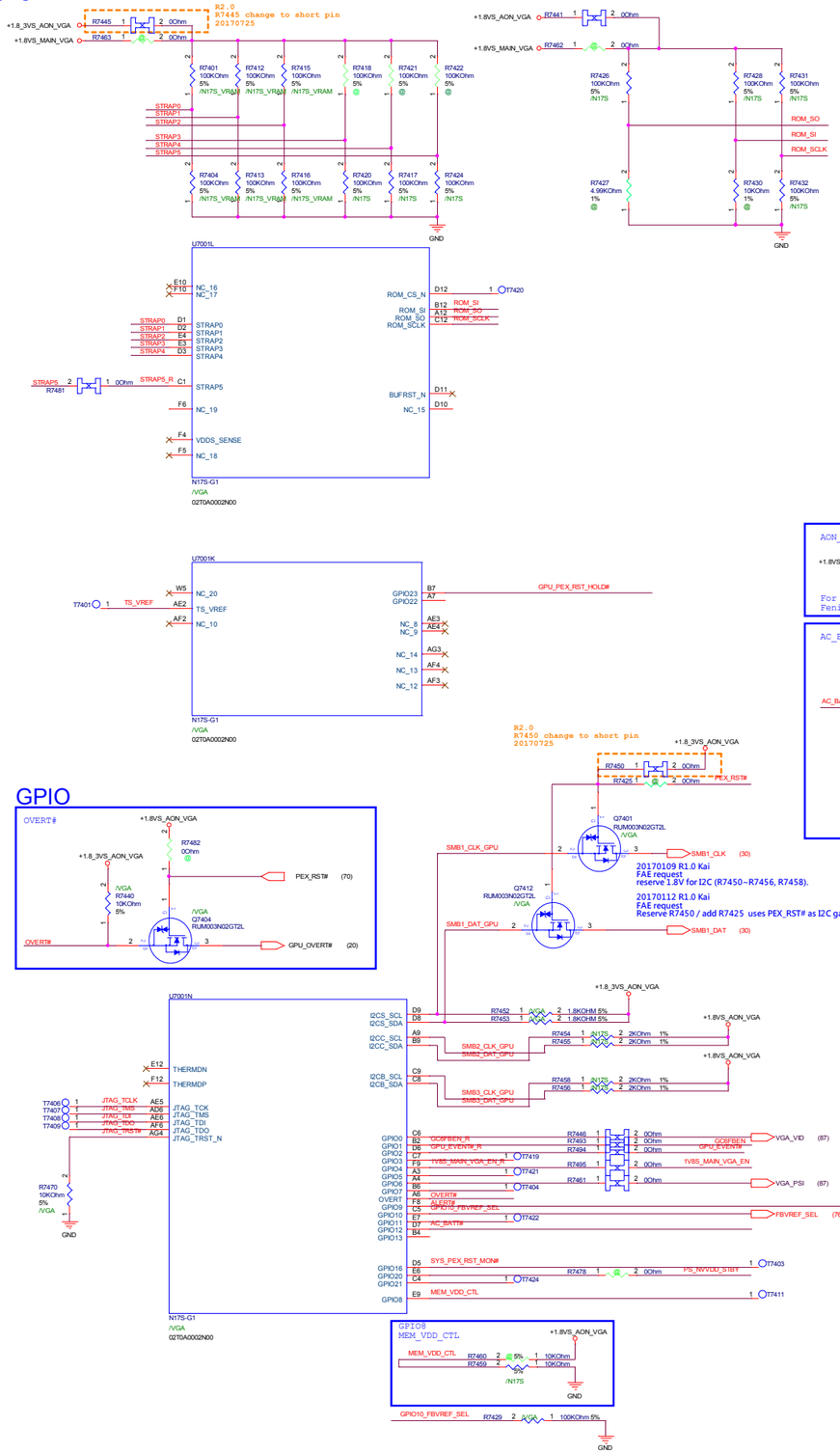
VBIOS ROM / Straping

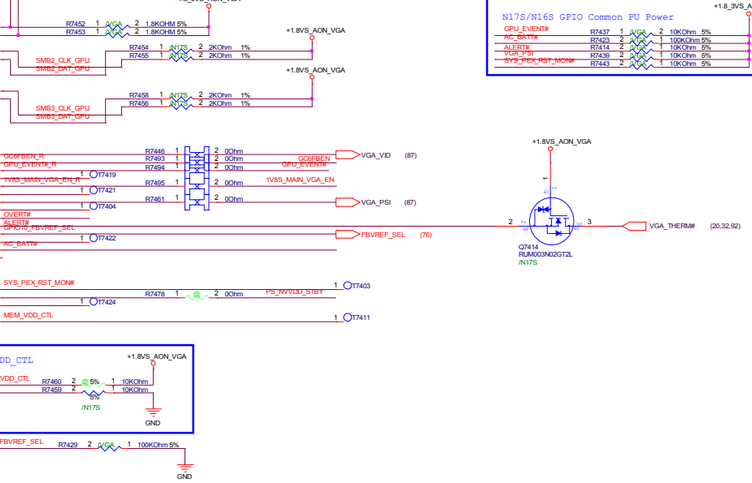
VGA_GPIO_STRAP



GPIO

20170109 R1.0 Kai
FAE request
reserve 1.8V for I2C (R7450~R7456, R7458).

20170112 R1.0 Kai
FAE request
Reserve R7450 / add R7425 uses PEX_RST# as I2C gate



From RVL-07916-001_v11 Table.4

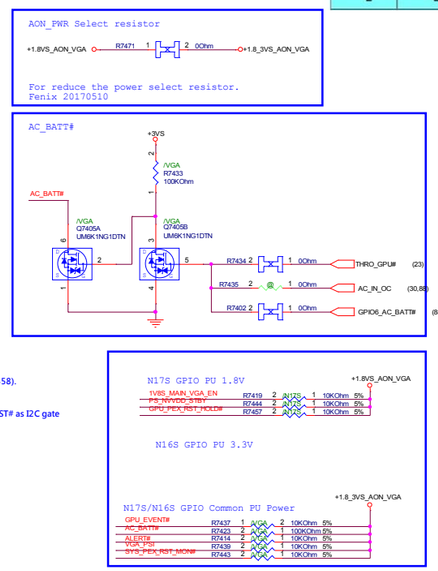
	GB2C-64(N17S-LG)	Vendor	Strap	STRAP2	STRAP1	STRAP0
	TBD	TBD	TBD			
	TBD	TBD	TBD			
0315-01SB0PB	H5GC8H24MJR-R0C	Hynix	0x2	L(R7416)	H(R7412)	L(R7404)
	TBD	TBD	TBD			
0315-02GE0PB	MT51J256M32HF-70:B	Micron	0x4	H(R7415)	L(R7413)	L(R7404)
0315-02GG0PB	H5GC8H24AJR-R0C	Hynix	0x5	H(R7415)	L(R7413)	H(R7401)
	TBD	TBD	TBD			
	TBD	TBD	TBD			
	TBD	TBD	TBD			

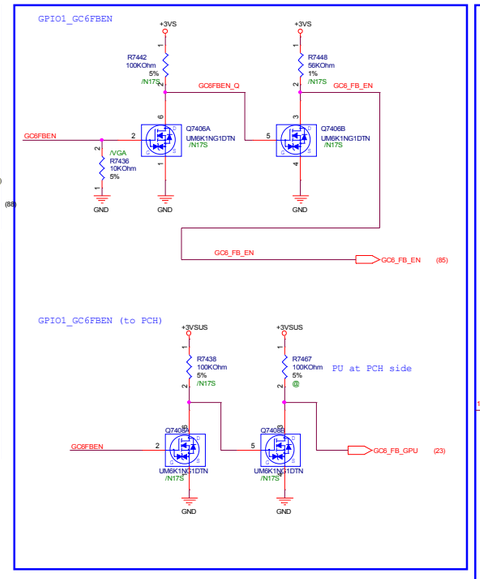
Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

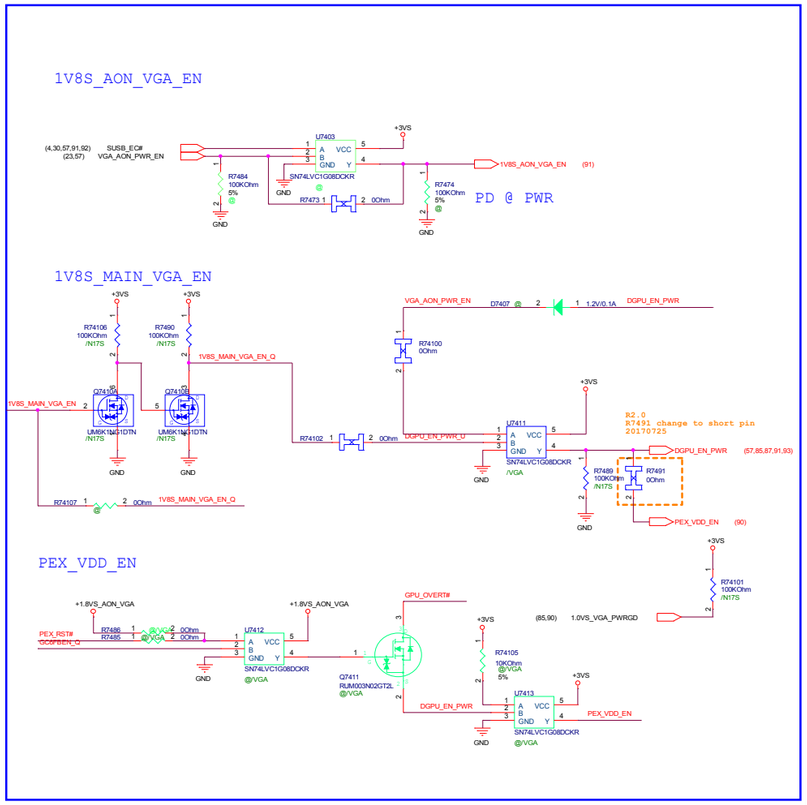
Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

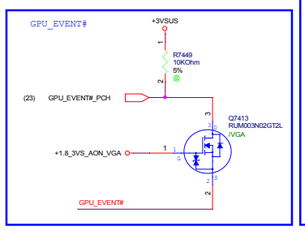
Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0









PEGATRON Title : VGA_GPIO,STRAP

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Howard Chen

BG1/4N1

Size	Project Name	Rev
D	MILLER	1.4

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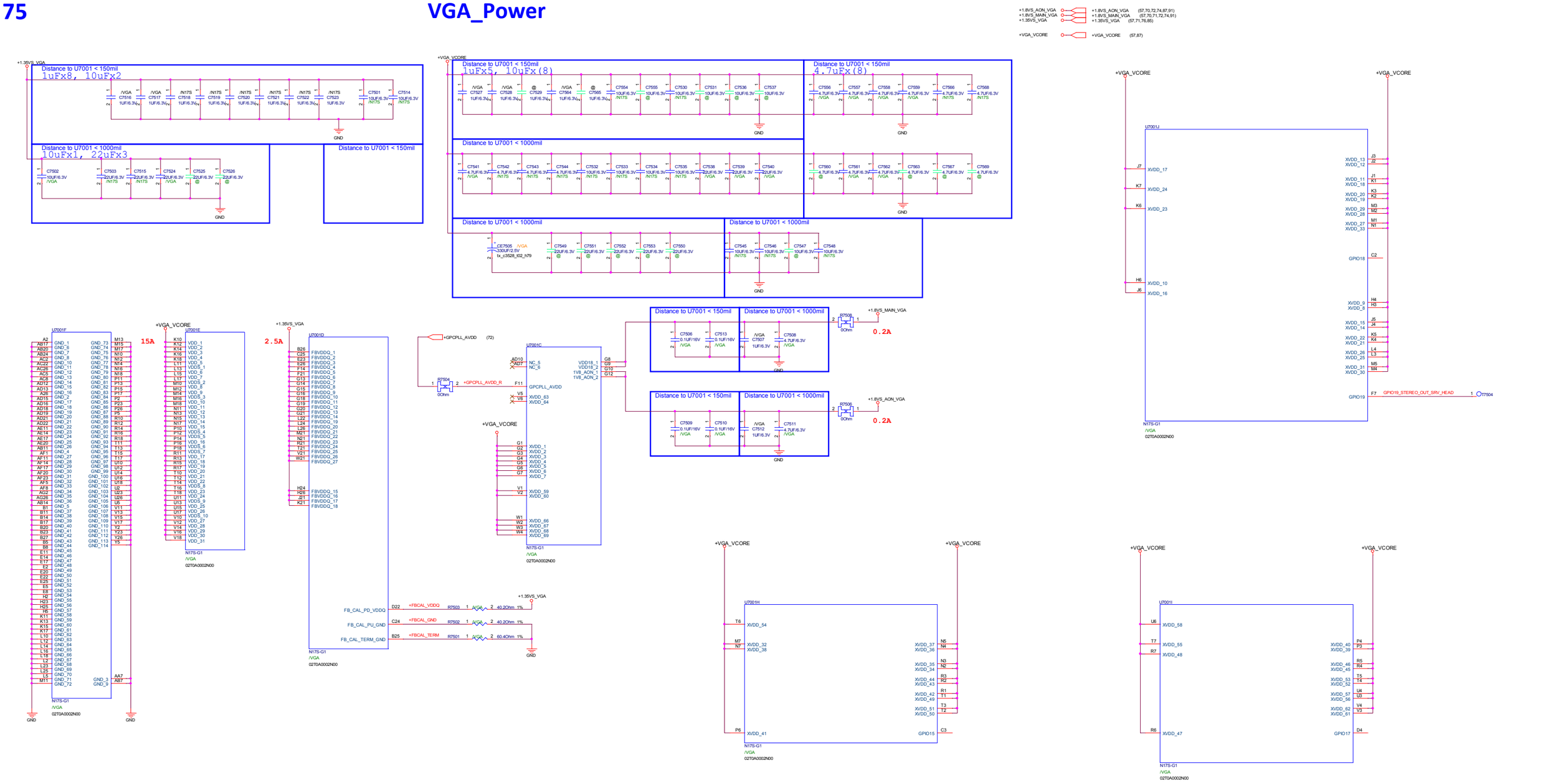
VGA_Power


+1.8VS_AON_VGA
+1.8VS_MAIN_VGA
+1.35VS_VGA
+VGA_VCORE
Distance to U7001 < 150mil
1uFx8, 10uFx2
Distance to U7001 < 1000mil
10uFx1, 22uFx3
Distance to U7001 < 150mil
1uFx5, 10uFx(8)
4.7uFx(8)
Distance to U7001 < 1000mil
U7001F
U7001E
U7001D
U7001C
U7001J
U7001H
U7001I
N17S-G1
/VGA
02T0A0002N00
15A
2.5A
0.2A
GND

VGA_FBA_GDDR5

nVidia Design Guide
DG-07875-001_v08 P.154
Table 9.5

	LOWER 0.31	UPPER 32..63
CMD0	CD#	
CMD1	A3,BA3	
CMD2	A2,BA2	
CMD3	A4,BA2	
CMD4	A5,BA1	
CMD5	RFF#	
CMD6	A6,A10	
CMD7	A8,A11	
CMD8	ABI#	
CMD9	A12,REF#	
CMD10	A9,A10	
CMD11	A7,A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CD#
CMD17		A3,BA3
CMD18		A2,BA2
CMD19		A4,BA2
CMD20		A5,BA1
CMD21		RFF#
CMD22		A7,A9
CMD23		A6,A11
CMD24		ABI#
CMD25		A12,REF#
CMD26		A9,A10
CMD27		A7,A9
CMD28		RST#
CMD29		CKE#
CMD30		CKE#
CMD31		CAS#

M1

3 : 24 ~ 31

2 : 16 ~ 23

1 : 8 ~15

0 : 0 ~ 7

U7601 — K4G80325FB-HC03

(71) FBAD[0..31]

(71) FBA_CMD[0..15]

(71) FBA_DBI[0..3]

(71) FBA_EDC[0..3]

(71) FBA_WCK01 / (71) FBA_WCK01#

(71) FBA_WCK23 / (71) FBA_WCK23#

(71) FBA_CLK0# / (71) FBA_CLK0

+1.35VS_VGA

20170216 R1.0 Gary
FAE suggest follow VRAM laout rule
Every SEN pin individual pull low
Add R7698 & R7699

R7601 1 2 /VGA 121OHM 1%
R7620 2 1 0Ohm

R7625 /VGA 1KOhm 1%

Non-Mirrored

R7613 549Ohm 1% — FAE confirm follow PSRCJ

R7606 1.33KOhm 1%

R7612 931OHM 1%

R7604 549Ohm 1% /VGA

R7616 931OHM 1% /VGA

R7617 1.33KOhm 1% /VGA

C7634 820PF/50V /VGA

C7631 820PF/50V /VGA

C7632 820PF/50V /VGA

FBA_VREFD

FBA_VREFC

FBA_VREF_FET

Q7601 RUM003N02GTZL /VGA

(74) FBVREF_SEL

FBA_CMD8

20170216 R1.0 Gary
FAE request follow N17S-G1 CRB

FBA_CLK0 — R7622 40.2Ohm 1% /VGA

FBA_CLK0# — R7623 40.2Ohm 1% /VGA — C7633 10NF/25V X7R/+/-5% /VGA

Place near U7601

/VGA C7606 1UF/6.3V; /VGA C7605 1UF/6.3V; /VGA C7604 1UF/6.3V; /VGA C7603 1UF/6.3V; /VGA C7602 1UF/6.3V; /VGA C7601 1UF/6.3V

/VGA C7607 1UF/6.3V; /N17S C7608 1UF/6.3V; /N17S C7609 1UF/6.3V; /N17S C7610 1UF/6.3V

C7611 10UF/6.3V /VGA; C7612 10UF/6.3V /VGA; C7613 10UF/6.3V /N17S; C7614 10UF/6.3V /N17S

Place around U7601

C7615 10UF/6.3V /N17S; C7616 10UF/6.3V /N17S; C7617 22UF/6.3V /N17S; C7618 22UF/6.3V /N17S

+1.35VS_VGA

92.0
Remove C7627 for layout modify
20170804

C7625 0.1UF/16V; C7626 0.1UF/16V; C7628 0.1UF/16V; C7629 0.1UF/16V; C7630 0.1UF/16V

Place below decoupling caps close VDD pin.
(Spare Capacitors)

M2

7 : 56 ~ 63

6 : 48 ~ 55

5 : 40 ~ 47

4 : 32 ~ 39

U7602 — K4G80325FB-HC03

(71) FBAD[32..63]

(71) FBA_CMD[16..31]

(71) FBA_DBI[4..7]

(71) FBA_EDC[4..7]

(71) FBA_WCK45 / (71) FBA_WCK45#

(71) FBA_WCK67 / (71) FBA_WCK67#

(71) FBA_CLK1# / (71) FBA_CLK1

R7640 1 2 /VGA 121OHM 1%
R7650 2 1 0Ohm

R7648 /VGA 1KOhm 1%

Non-Mirrored

C7673 820PF/50V X7R/+/-10%

C7640 820PF/50V X7R/+/-10%

C7641 820PF/50V /VGA

FBA_VREFD

FBA_VREFC

FBA_CMD24

FBA_CLK1

R7649 40.2Ohm 1% /VGA

R7651 40.2Ohm 1% /VGA

C7650 10NF/25V X7R/+/-5% /VGA

FBA_CLK1#

Place near U7602

/VGA C7657 1UF/6.3V; /VGA C7654 1UF/6.3V; /VGA C7655 1UF/6.3V; /VGA C7658 1UF/6.3V; /VGA C7656 1UF/6.3V; /VGA C7656 1UF/6.3V

/VGA C7642 1UF/6.3V; /N17S C7644 1UF/6.3V; /N17S C7646 1UF/6.3V; /N17S C7653 1UF/6.3V

C7652 10UF/6.3V /VGA; C7644 10UF/6.3V /VGA; C7650 10UF/6.3V /N17S; C7647 10UF/6.3V /N17S

Place around U7602

C7648 10UF/6.3V /VGA; C7649 10UF/6.3V /VGA; C7643 22UF/6.3V /N17S; C7645 22UF/6.3V /N17S

+1.35VS_VGA

C7667 0.1UF/16V; C7668 0.1UF/16V; C7669 0.1UF/16V; C7670 0.1UF/16V; C7671 0.1UF/16V; C7672 0.1UF/16V

Place below decoupling caps close VDD pin.
(Spare Capacitors)

PEGATRON Title : VGA_FBA_GDDR5-1
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Howard Chen
BG1/MW1
Size D | Project Name MILLER | Rev 1.4
Date: Monday, June 11, 2018 Sheet 76 of 94

5 4 3 2 1

D C B A

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName>

Engineer: Howard Chen

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

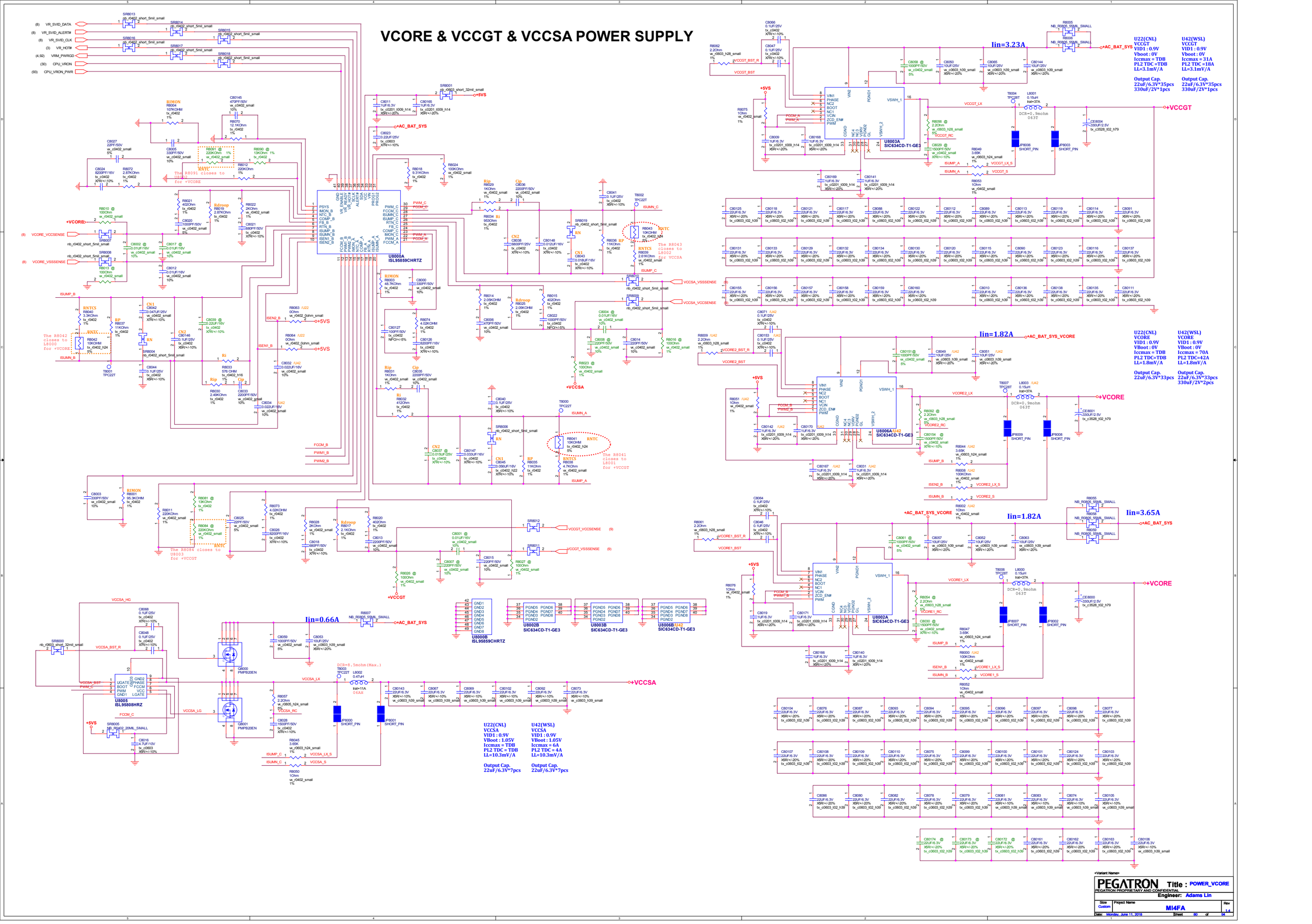
<OrgName>

Engineer: Howard Chen

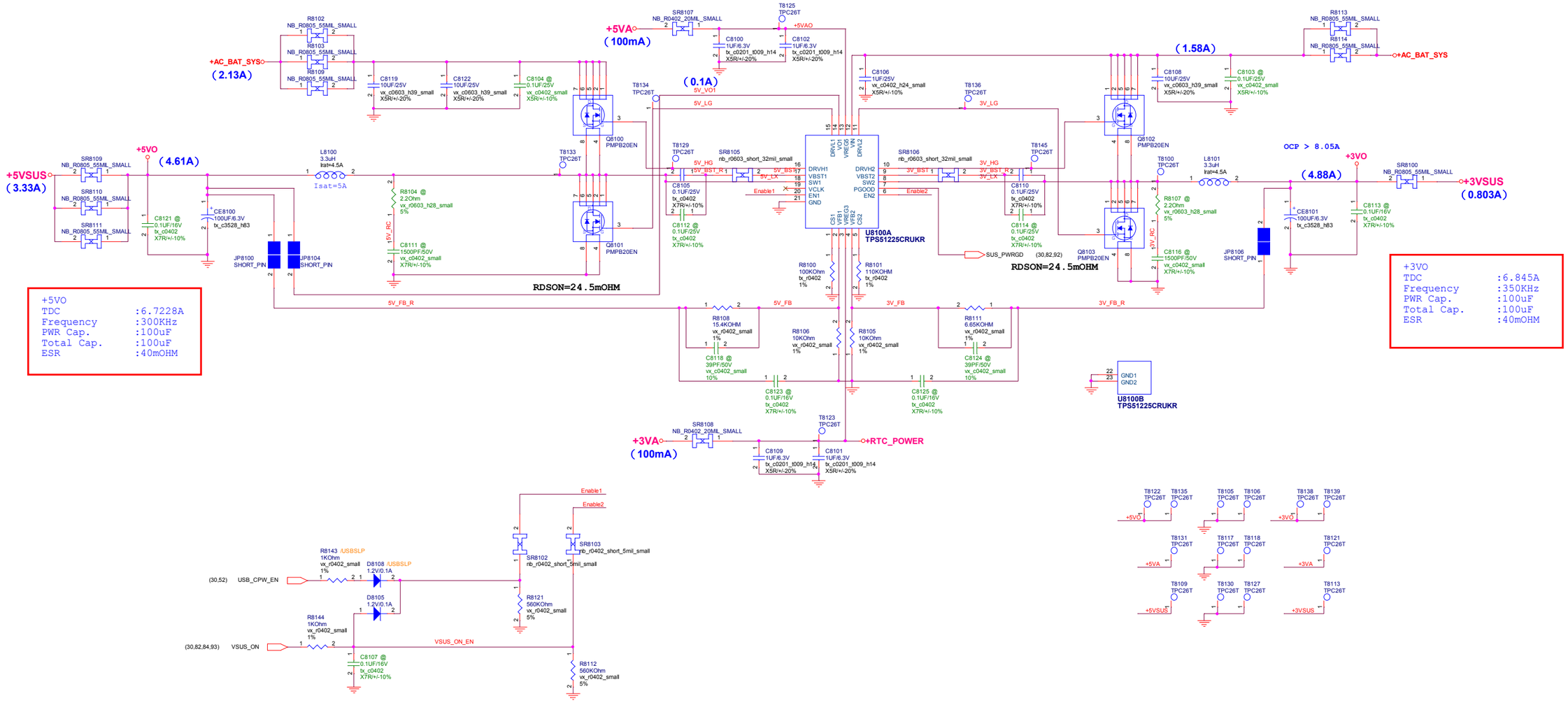
Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

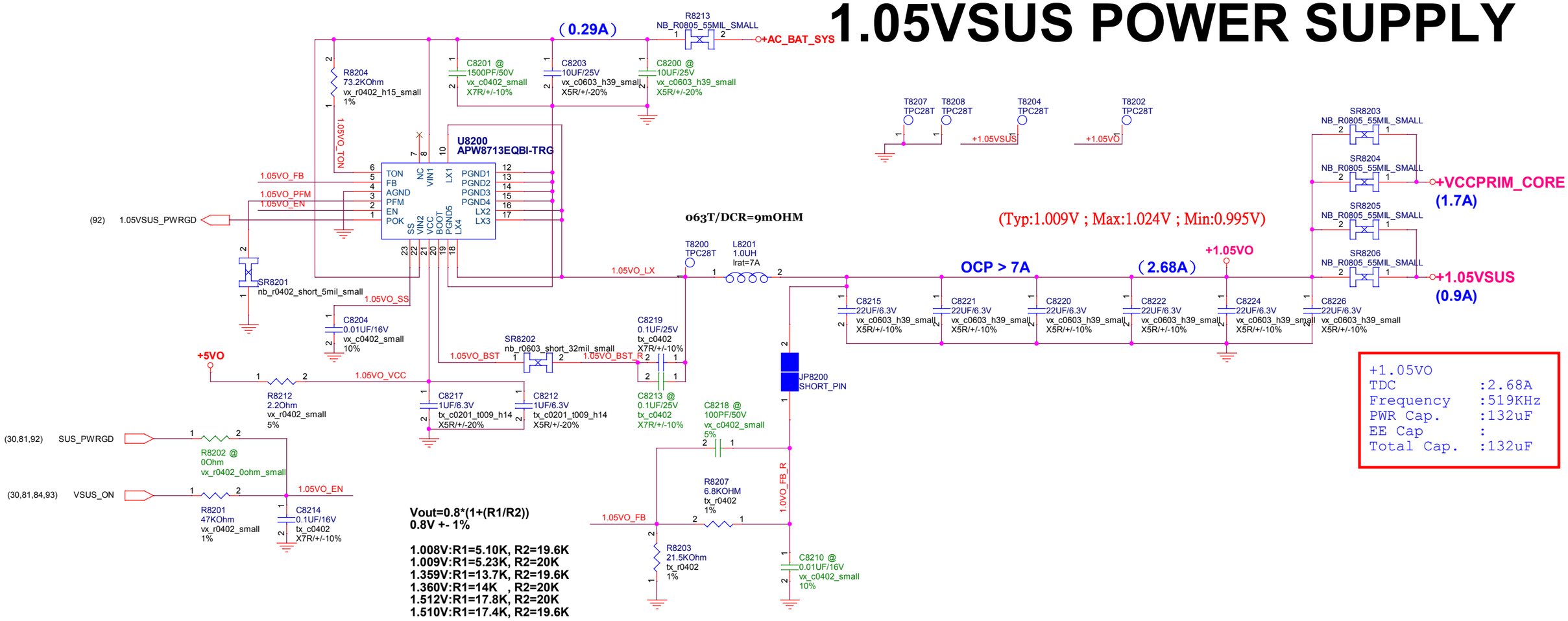
VCORE & VCCGT & VCCSA POWER SUPPLY



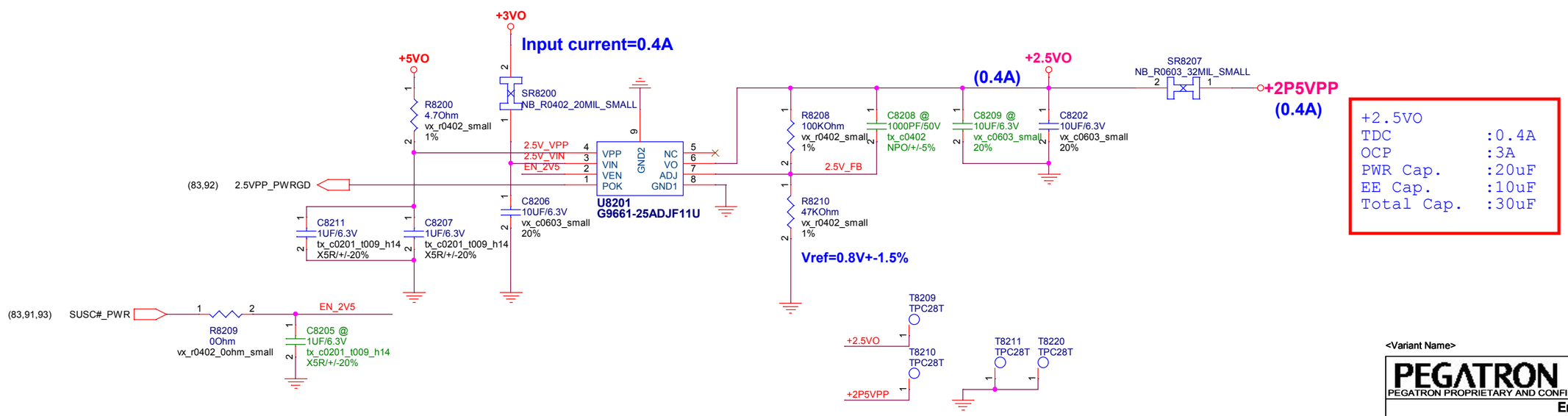
5VO & 3VO POWER SUPPLY



1.05VSUS POWER SUPPLY



2.5V POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

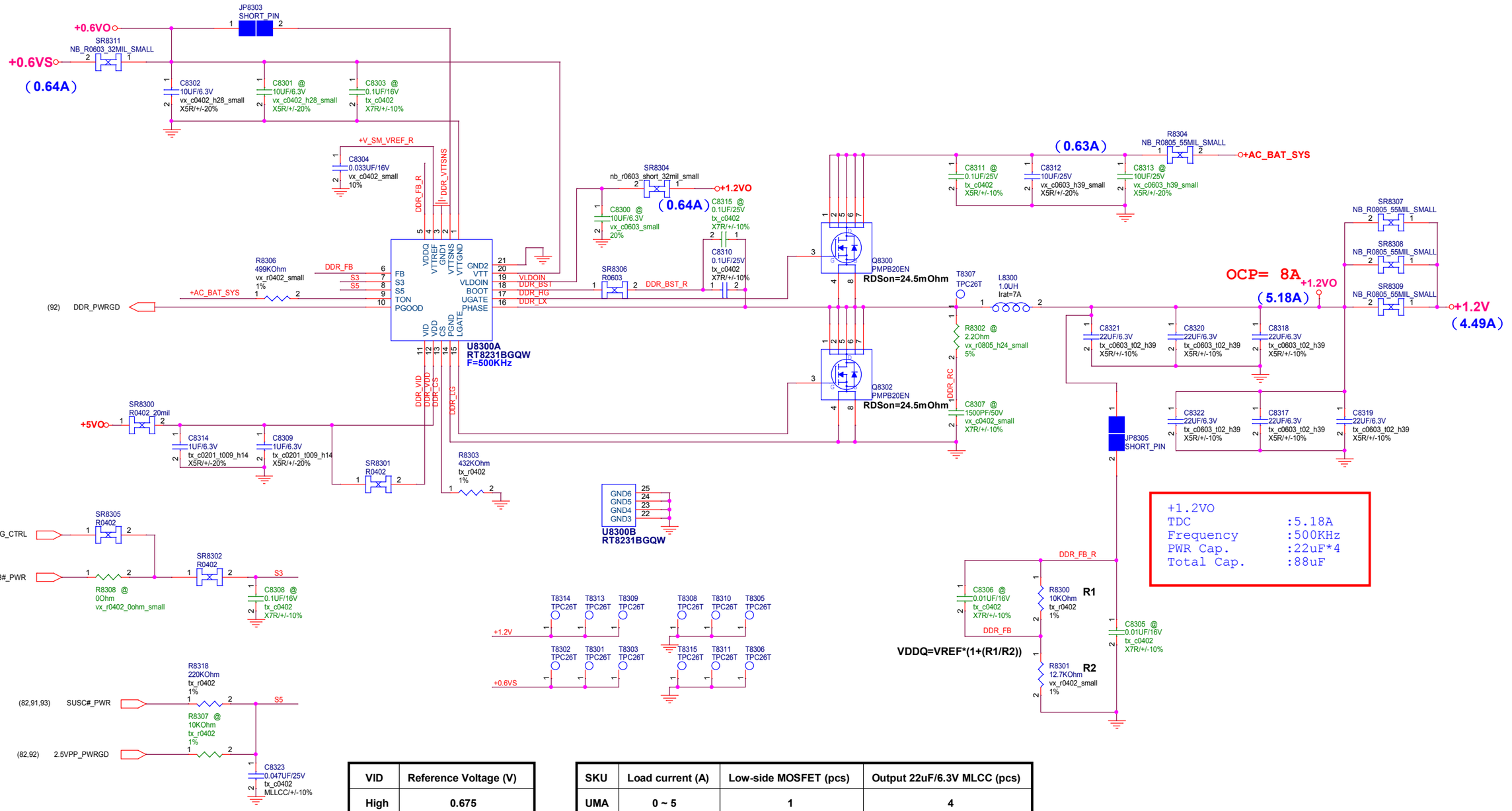
Title : PWR_+1.0VSUS & +2.5V

Engineer: Adams Lin

Size	Project Name	Rev
Custom	MI4FA	1.4

Date: Monday, June 11, 2018 Sheet 82 of 94

DDR & VTT POWER SUPPLY



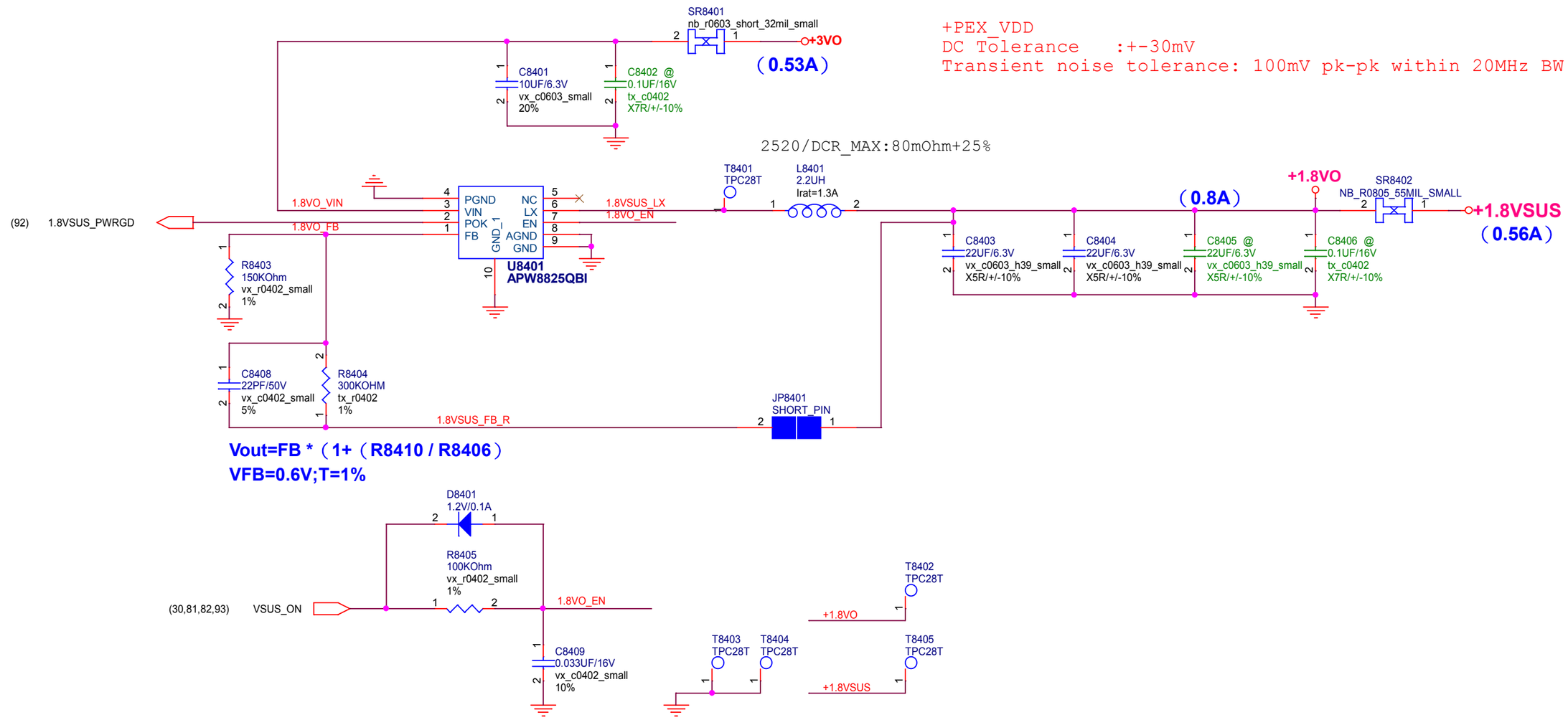
+1.2VO
TDC :5.18A
Frequency :500KHz
PWR Cap. :22uF*4
Total Cap. :88uF

VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_DDR & VTT
Engineer: Adams Lin
BG1-POWER
Size Custom
Project Name MI4FA
Rev 1.4
Date: Monday, June 11, 2018
Sheet 83 of 94

1.8VSUS POWER SUPPLY



+PEX_VDD
DC Tolerance :+-30mV
Transient noise tolerance: 100mV pk-pk within 20MHz BW

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

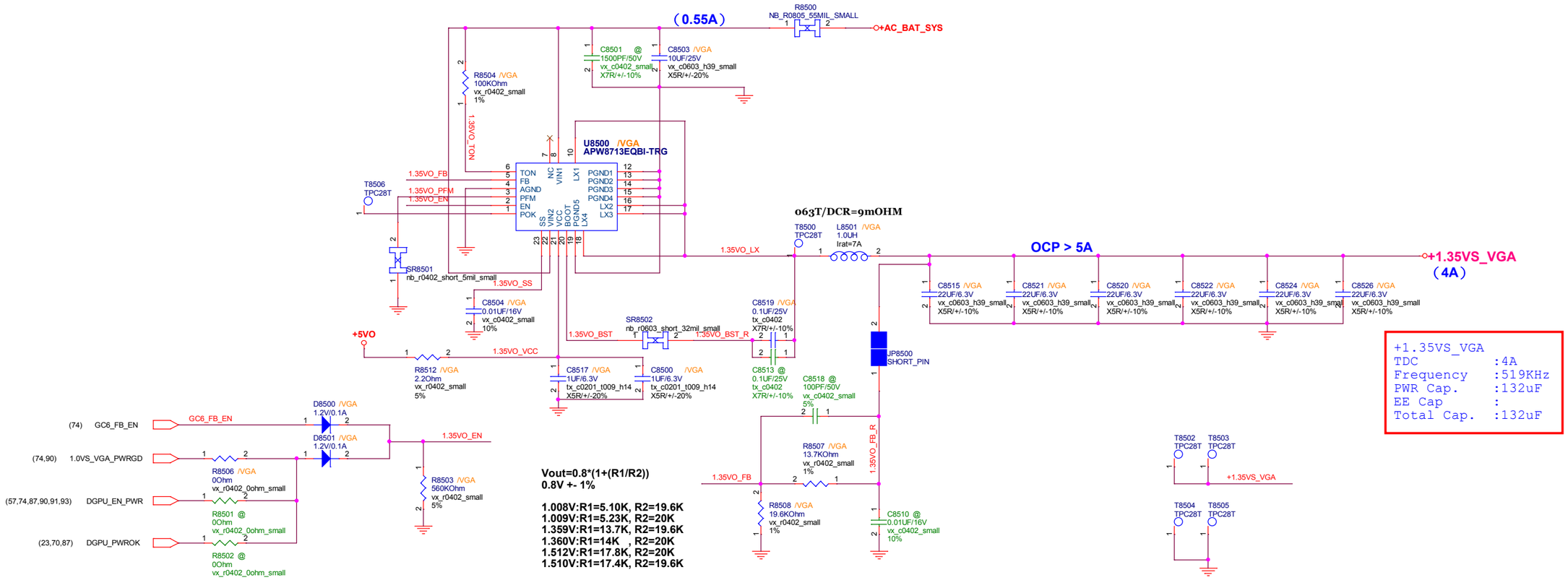
Title : POWER_+1.8VSUS

Engineer: Adams Lin

Size	Project Name	Rev
B	MI4FA	1.4

Date: Monday, June 11, 2018 Sheet 84 of 94

1.35VS_VGA POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_1.35VS_VGA

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Adams Lin

Size	Project Name	Rev
Custom	MI4FA	1.4

Date: Monday, June 11, 2018 Sheet 85 of 94

PEGATRON

Title : RSVD

PEGATRON PROPRIETARY AND CONFIDENTIAL

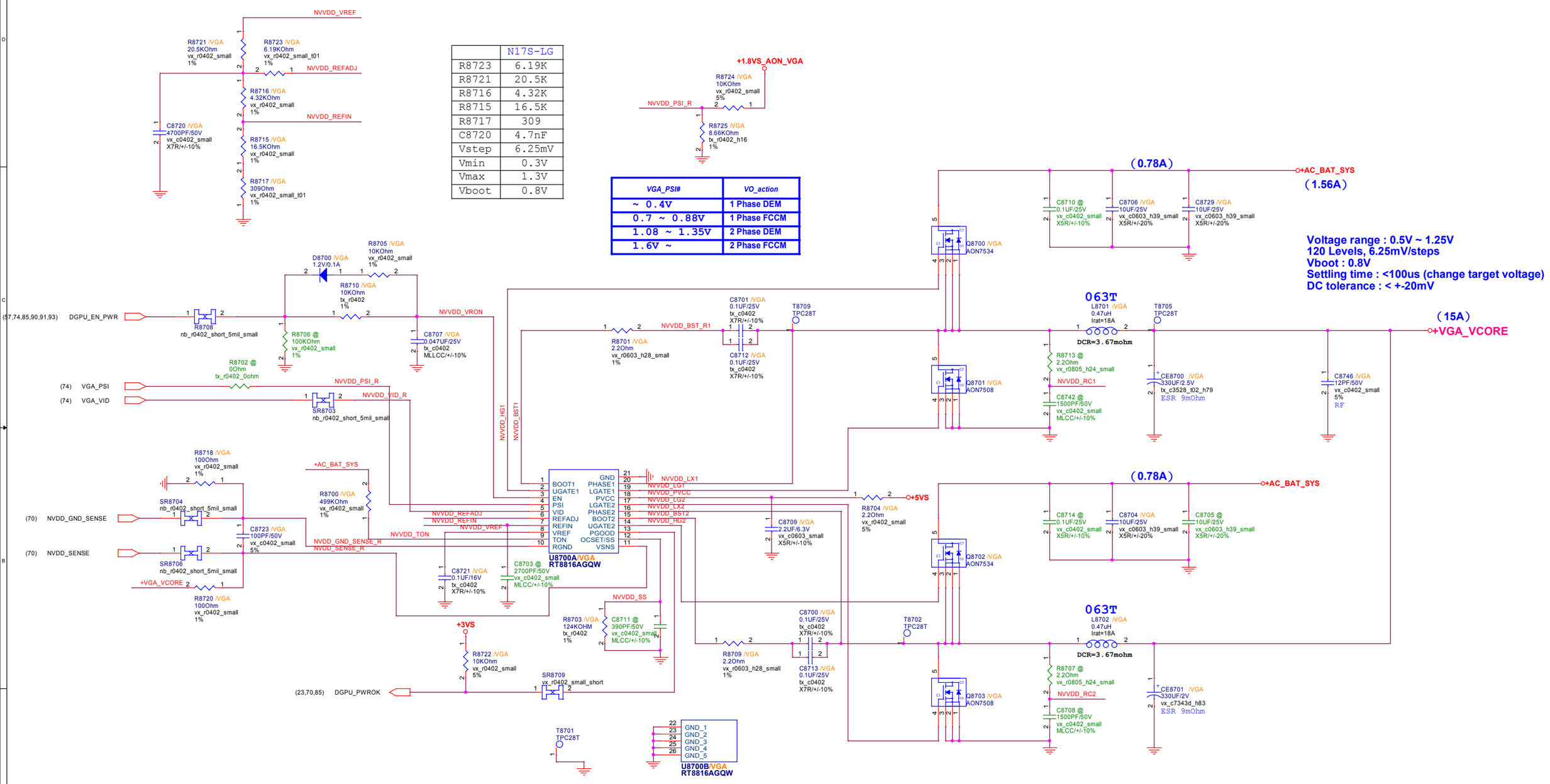
<OrgName>

Engineer: Adams Lin

Size	Project Name	Rev
A	MILLER	1.4

Date: Monday, June 11, 2018

VGA_CORE POWER SUPPLY



	N17S-LG
R8723	6.19K
R8721	20.5K
R8716	4.32K
R8715	16.5K
R8717	309
C8720	4.7nF
Vstep	6.25mV
Vmin	0.3V
Vmax	1.3V
Vboot	0.8V

VGA_PSI#	VO_action
~ 0.4V	1 Phase DEM
0.7 ~ 0.88V	1 Phase FCCM
1.08 ~ 1.35V	2 Phase DEM
1.6V ~	2 Phase FCCM

Voltage range : 0.5V ~ 1.25V
120 Levels, 6.25mV/steps
Vboot : 0.8V
Settling time : <100us (change target voltage)
DC tolerance : < +-20mV

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

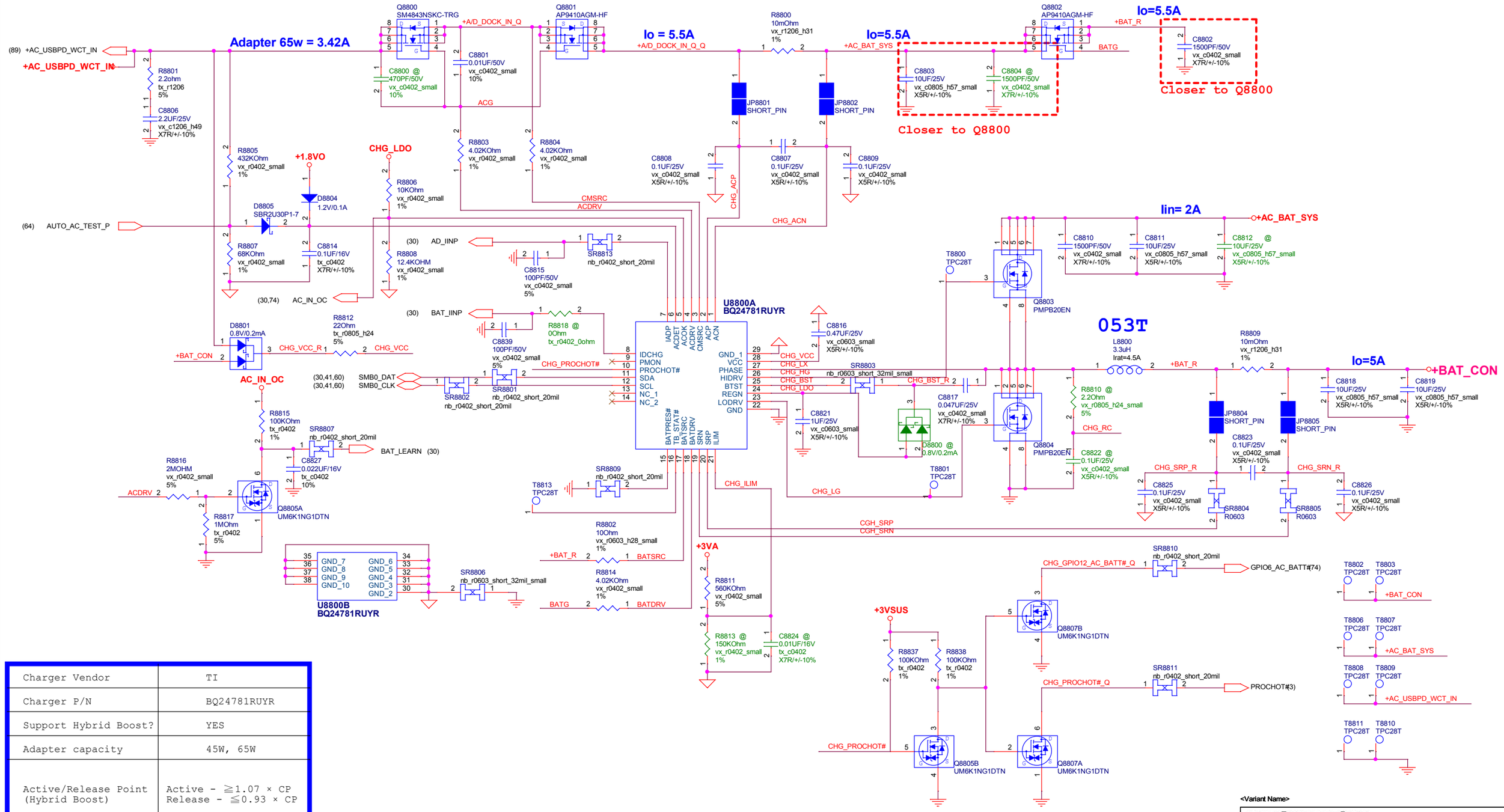
Title : POWER_VGA

Engineer: Adams Lin

Size	Project Name	Rev
Custom	MI4FA	1.4

Date: Monday, June 11, 2018 Sheet 87 of 94

BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24781RUYR
Support Hybrid Boost?	YES
Adapter capacity	45W, 65W
Active/Release Point (Hybrid Boost)	Active - ≧1.07 × CP Release - ≦0.93 × CP
Enable condition Disable condition	RSOC≧40% RSOC≦30%

<Variant Name>

PEGATRON Title : POWER_CHARGER

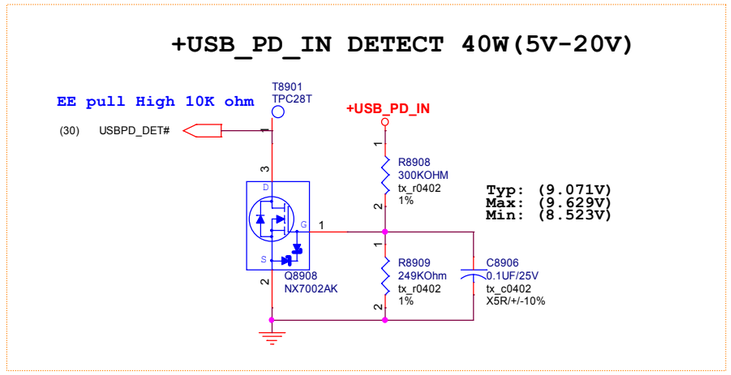
PEGATRON PROPRIETARY AND CONFIDENTIAL

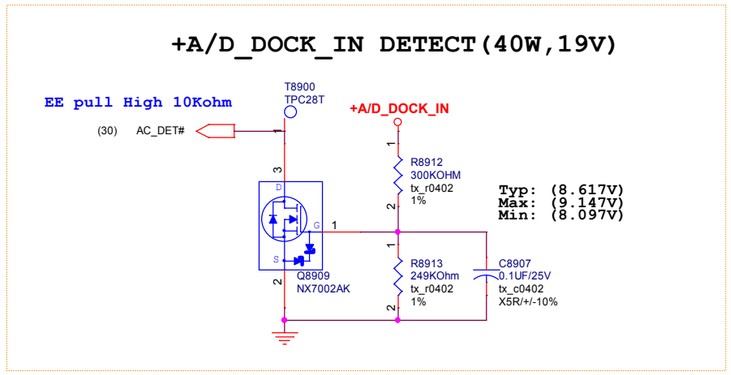
Engineer: Adams Lin

Size	Project Name	Rev
Custom	MI4FA	1.4

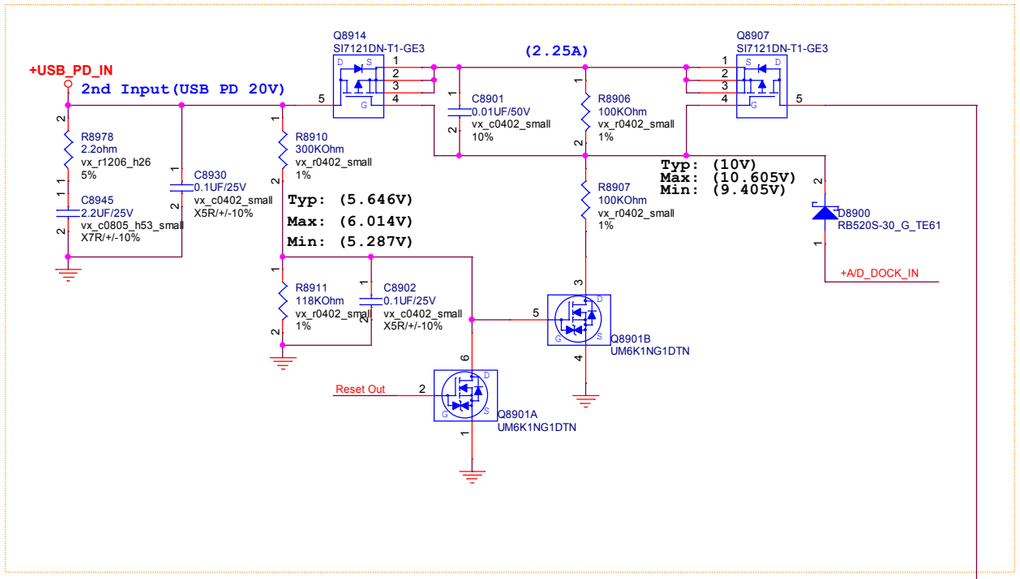
Date: Monday, June 11, 2018 Sheet 88 of 94

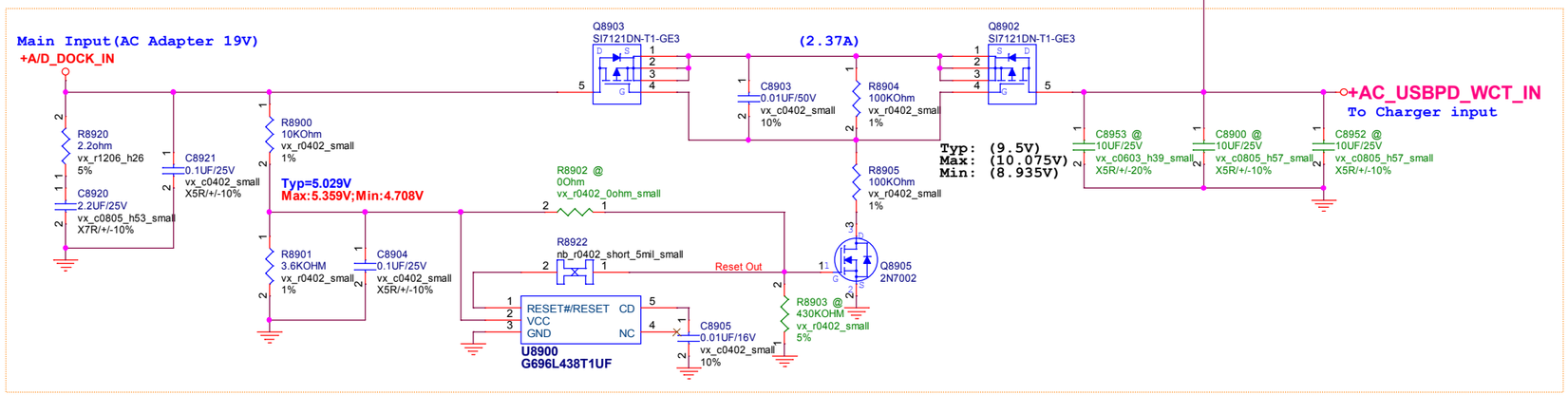
AC & USB_PD Detect





2 Input switch Circuit





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

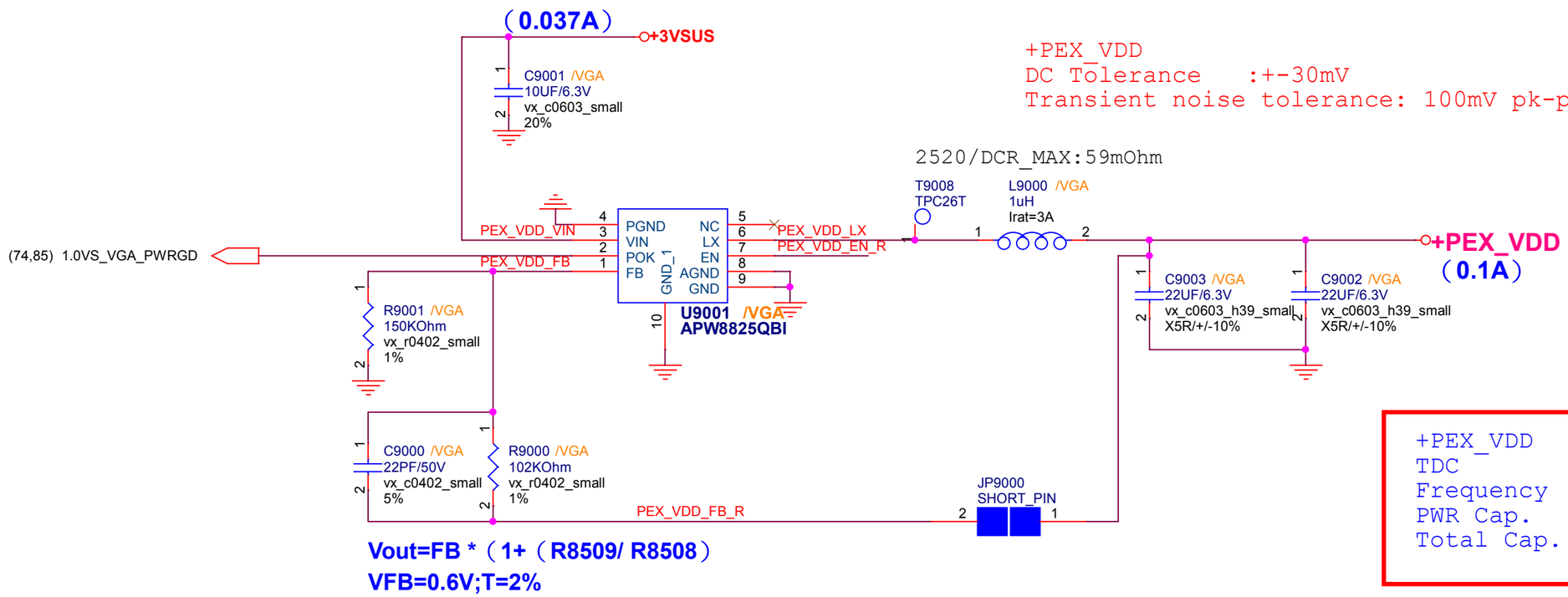
Title : AC&PD S.W.

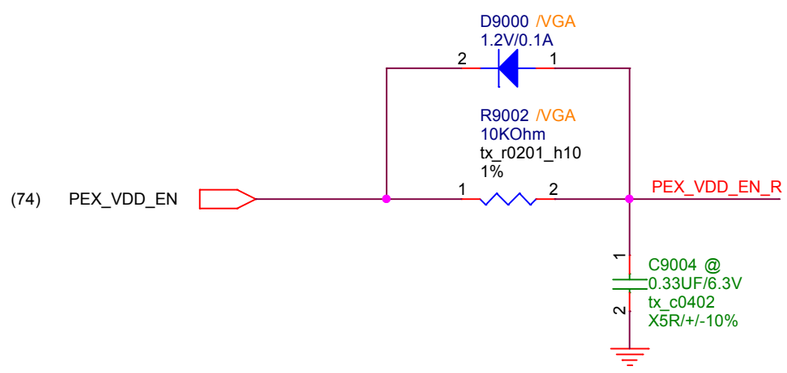
Engineer: Adams Lin

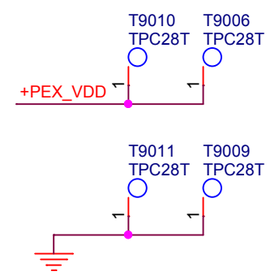
Size	Project Name	Rev
Custom	MI4FA	1.4

Date: Monday, June 11, 2018 Sheet 89 of 94

PEX_VDD POWER SUPPLY







<Variant Name>

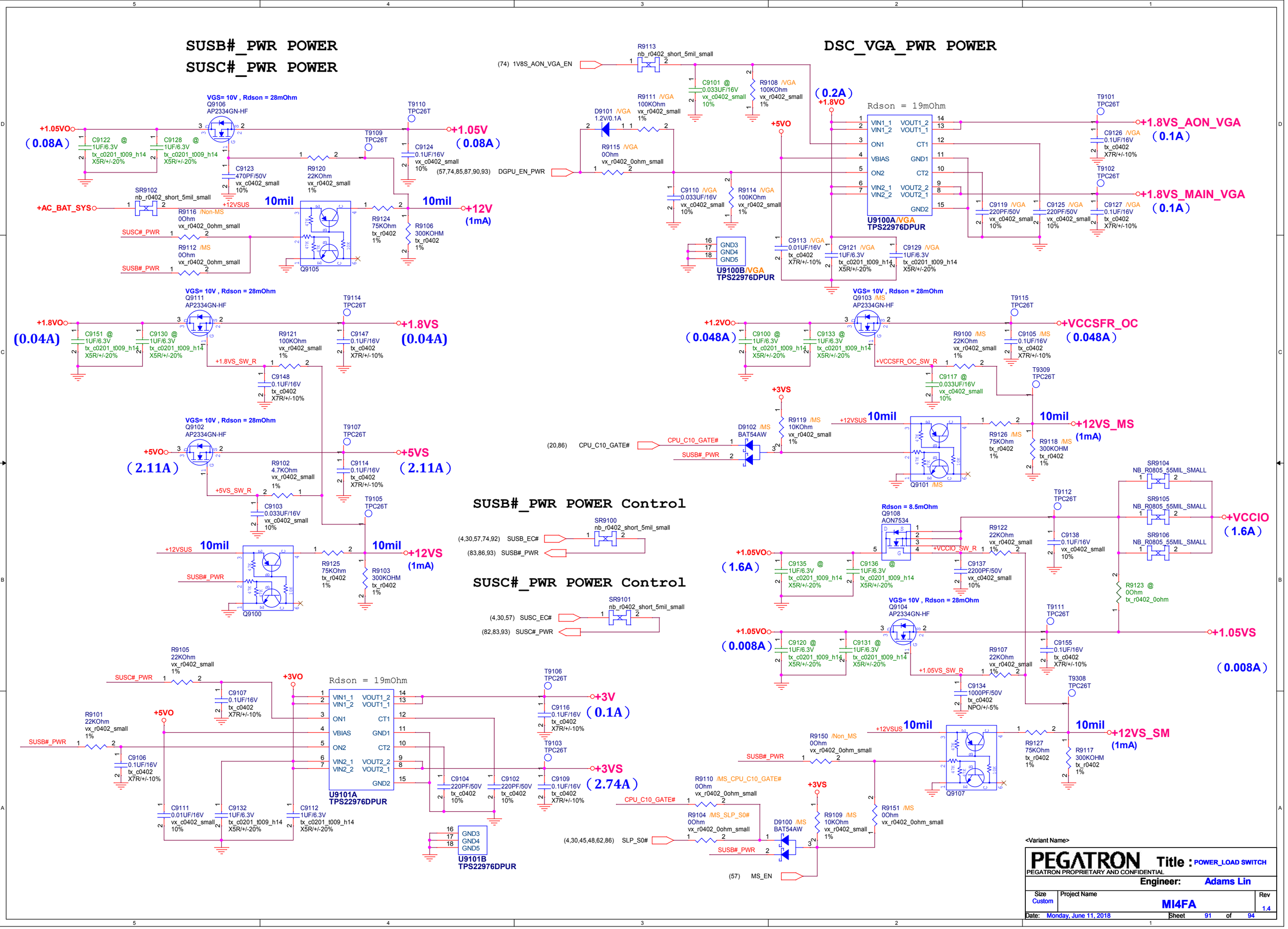
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : PWR_PEX_VDD

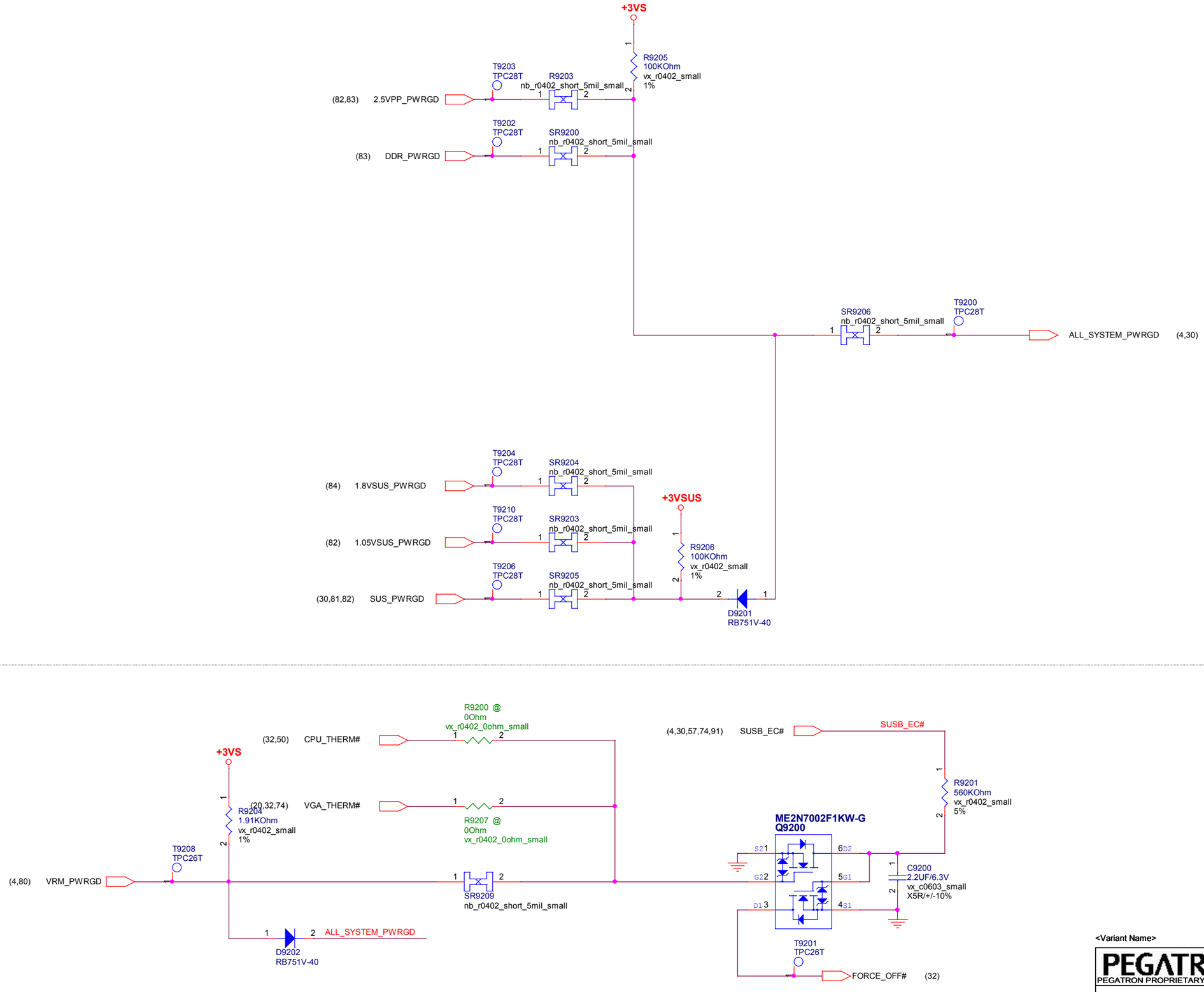
Engineer: Adams Lin

Size	Project Name	Rev
Custom	MI4FA	1.4

Date: Monday, June 11, 2018 Sheet 90 of 94


SUSB#_PWR POWER
SUSC#_PWR POWER
DSC_VGA_PWR POWER
SUSB#_PWR POWER Control
SUSC#_PWR POWER Control
+1.05VO
(0.08A)
Q9106
AP2334GN-HF
VGS= 10V , Rdson = 28mOhm
T9110
TPC26T
T9109
TPC26T
+1.05V
(0.08A)
+AC_BAT_SYS
SR9102
+12VSUS
10mil
+12V
(1mA)
R9116 /Non-MS
SUSC#_PWR
R9112 /MS
SUSB#_PWR
Q9105
R9120
22KOhm
R9124
75KOhm
R9106
300KOHM
(57,74,85,87,90,93) DGPU_EN_PWR
(74) 1V8S_AON_VGA_EN
R9113
nb_r0402_short_5mil_small
R9111 /VGA
100KOhm
D9101 /VGA
1.2V/0.1A
R9115 /VGA
0Ohm
R9108 /VGA
100KOhm
(0.2A)
+1.8VO
+5VO
Rdson = 19mOhm
U9100A/VGA
TPS22976DPUR
U9100B/VGA
TPS22976DPUR
T9101
TPC26T
+1.8VS_AON_VGA
(0.1A)
T9102
TPC26T
+1.8VS_MAIN_VGA
(0.1A)
+1.8VO
(0.04A)
Q9111
AP2334GN-HF
T9114
TPC26T
+1.8VS
(0.04A)
+1.8VS_SW_R
R9121
100KOhm
+5VO
(2.11A)
Q9102
AP2334GN-HF
T9107
TPC26T
+5VS
(2.11A)
+5VS_SW_R
R9102
4.7KOhm
T9105
TPC26T
+12VSUS
10mil
+12VS
(1mA)
SUSB#_PWR
Q9100
R9125
75KOhm
R9103
300KOHM
(4,30,57,74,92) SUSB_EC#
(83,86,93) SUSB#_PWR
SR9100
(4,30,57) SUSC_EC#
(82,83,93) SUSC#_PWR
SR9101
+1.2VO
(0.048A)
Q9103 /MS
AP2334GN-HF
T9115
TPC26T
+VCCSFR_OC
(0.048A)
+VCCSFR_OC_SW_R
R9100 /MS
22KOhm
T9309
TPC26T
+3VS
D9102 /MS
BAT54AW
R9119 /MS
10KOhm
(20,86) CPU_C10_GATE#
CPU_C10_GATE#
SUSB#_PWR
+12VSUS
10mil
+12VS_MS
(1mA)
R9126 /MS
75KOhm
R9118 /MS
300KOHM
Q9101 /MS
Rdson = 8.5mOhm
Q9108
AON7534
+1.05VO
(1.6A)
+VCCIO_SW_R
R9122
22KOhm
T9112
TPC26T
SR9104
NB_R0805_55MIL_SMALL
SR9105
NB_R0805_55MIL_SMALL
SR9106
NB_R0805_55MIL_SMALL
+VCCIO
(1.6A)
R9123 @
0Ohm
VGS= 10V , Rdson = 28mOhm
Q9104
AP2334GN-HF
T9111
TPC26T
+1.05VO
(0.008A)
+1.05VS
(0.008A)
+1.05VS_SW_R
R9107
22KOhm
T9308
TPC26T
+12VSUS
10mil
+12VS_SM
(1mA)
R9150 /Non_MS
SUSB#_PWR
Q9107
R9127
75KOhm
R9117
300KOHM
R9105
22KOhm
SUSC#_PWR
+3VO
Rdson = 19mOhm
R9101
22KOhm
+5VO
SUSB#_PWR
U9101A
TPS22976DPUR
U9101B
TPS22976DPUR
T9106
TPC26T
+3V
(0.1A)
T9103
TPC26T
+3VS
(2.74A)
R9110 /MS_CPU_C10_GATE#
CPU_C10_GATE#
R9104 /MS_SLP_S0#
(4,30,45,48,62,86) SLP_S0#
D9100 /MS
BAT54AW
R9109 /MS
10KOhm
R9151 /MS
(57) MS_EN
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_LOAD SWITCH
Engineer: Adams Lin
Size Custom
Project Name MI4FA
Rev 1.4
Date: Monday, June 11, 2018
Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

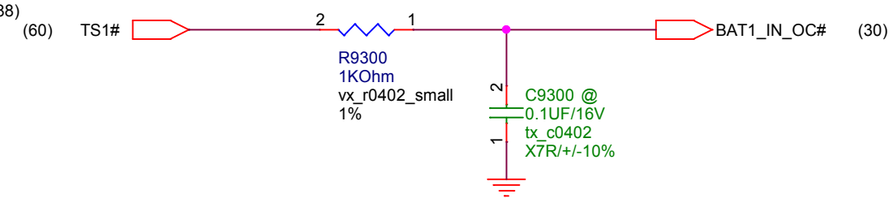
Title : POWER_PROTECT

Engineer: Adams Lin

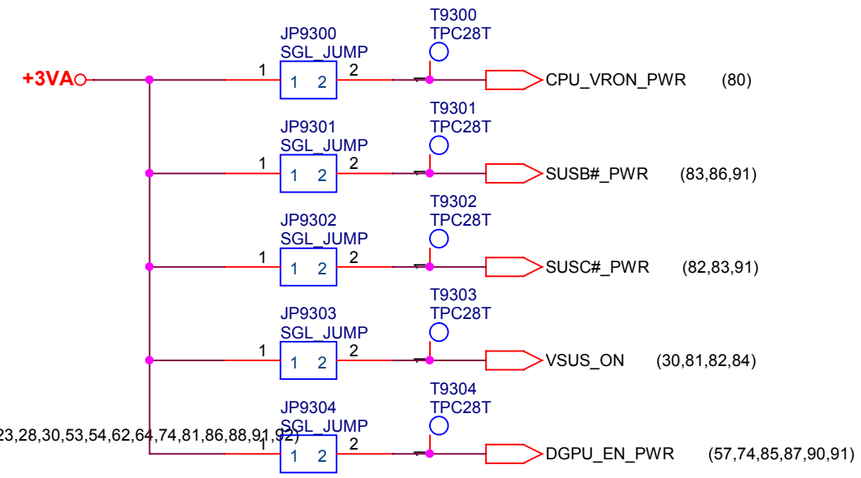
Size	Project Name	Rev
Custom	MI4FA	1.4

Date: Monday, June 11, 2018 Sheet 92 of 94

BATTERY IN DETECT



FOR POWER TEST



+AC_USBPD_WCT_IN	+AC_USBPD_WCT_IN	(88,89)
+A/D_DOCK_IN	+A/D_DOCK_IN	(60,89)
+USB_PD_IN	+USB_PD_IN	(42,89)
+AC_BAT_SYS	+AC_BAT_SYS	(41,43,45,80,81,82,83,85,87,88)
+BAT_CON	+BAT_CON	(60,88)
+RTC_POWER	+RTC_POWER	(81)
+5VA	+5VA	(64,81)
+3VA	+3VA	(21,30,31,36,43,57,64,81,88)
+5VO	+5VO	(81,82,83,85,90,91)
+3VO	+3VO	(81,82,84,86,90,91)
+2.5VO	+2.5VO	(82)
+1.8VO	+1.8VO	(84,88,91)
+1.2VO	+1.2VO	(83,91)
+1.05VO	+1.05VO	(82,91)
+0.6VO	+0.6VO	(83)
+5VSUS	+5VSUS	(41,42,52,64,81)
+3VSUS	+3VSUS	(3,4,6,10,20,21,22,23,28,30,53,54,62,64,74,81,86,88,91,92)
+1.8VSUS	+1.8VSUS	(10,21,23,84)
+1.05VSUS	+1.05VSUS	(10,82)
+2P5VPP	+2P5VPP	(16,17,57,82)
+1.2V	+1.2V	(6,9,15,16,17,19,57,83)
+1.05V	+1.05V	(9,32,57,91)
+5VS	+5VS	(31,36,45,48,50,57,69,80,87,91)
+3VS	+3VS	(3,4,6,20,21,23,30,32,36,41,42,44,45,48,50,51,53,57,62,64,74,87,91,92)
+1.8VS	+1.8VS	(36,57,91)
+0.6VS	+0.6VS	(15,57,83)
+VCORE	+VCORE	(8,9,80)
+VCCGT	+VCCGT	(9,80)
+VCCSA	+VCCSA	(9,80)
+VCCIO	+VCCIO	(3,9,57,86)
+VCCPRIM_CORE	+VCCPRIM_CORE	(10,82)
+VGA_VCORE	+VGA_VCORE	(57,75,87)
+1.05VS	+1.05VS	(9,57,91)
+AC_BAT_SYS_VCORE	+AC_BAT_SYS_VCORE	(80)
+1.8VS_AON_VGA	+1.8VS_AON_VGA	(57,70,72,74,75,87,91)
+1.8VS_MAIN_VGA	+1.8VS_MAIN_VGA	(57,70,71,72,74,75,91)
+1.35VS_VGA	+1.35VS_VGA	(57,71,75,76,85)
+PEX_VDD	+PEX_VDD	(57,70,90)

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

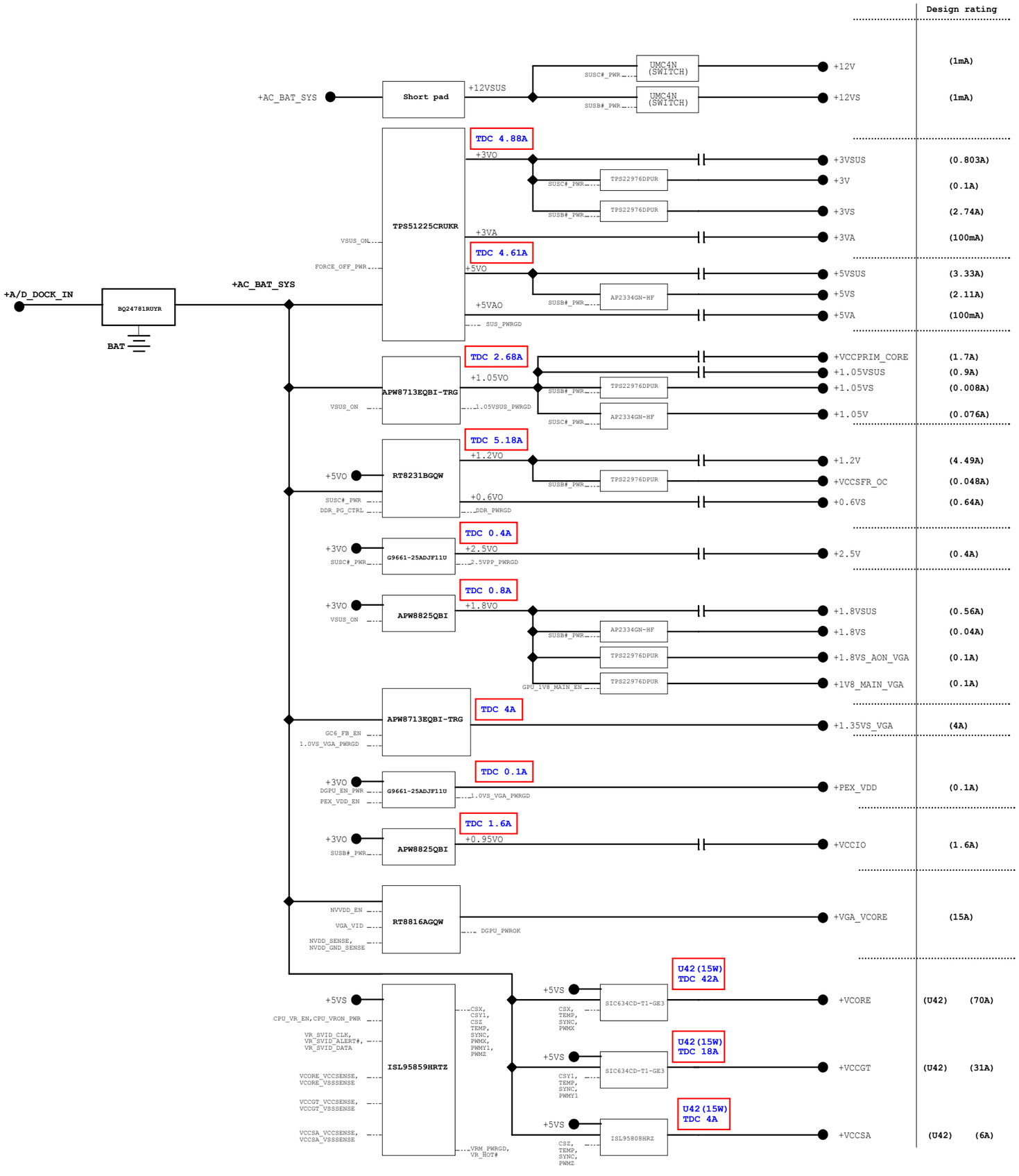
Title : PWR_SIGNAL & DETECT

BG1-POWER

Engineer: Adams Lin

Size	Project Name	Rev
Custom	MI4FA	1.4

Date: Monday, June 11, 2018 Sheet 93 of 94



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_FLOWCHART

Engineer: Adams Lin

Size	Project Name	Rev
Custom	MI4FA	1.4

Date: Monday, June 11, 2018 Sheet 94 of 99